PRO-LOG®
CORPORATION

STD 7000

7864
Multimaster 8088
CPU/SBX Card

USER'S MANUAL

10/85

FOREWORD

This manual explains how to use Pro-Log's 7864 Multimaster 8088 CPU/SBX card. It is structured to reflect the answers to basic questions about the 7864. We welcome your suggestions on how we can improve our instructions.

The 7864 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and provide industrial managers with the means of using their own people to control the design, production, and maintenance of products that use STD BUS hardware. Pro-Log also offers applications seminars based on STD BUS products.

Our products are designed to quality standards with readily available, second-sourced, industry standard components, clear and complete specifications, full documentation, and the option to purchase the manufacturing rights and drawings.

You may also find the *STD BUS Technical Manual* useful in your work. If you would like a copy of this document, please write to us on your company letterhead.

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Section 1
SPECIFICATIONS

PURPOSE

The 7864 is a multifunction 8088 CPU card with up to 128K of onboard memory, SBX connectors for two user-supplied SBX I/O expansion modules, an 8259A interrupt controller, an 8253-5 counter/timer, and an optional 8087 math coprocessor.

Specially designed bus arbitration logic allows the use of more than one 7864 (or other Pro-Log multimaster CPU cards) in one STD BUS backplane, each with access to global memory and I/O (i.e., memory and I/O not located on a multimaster CPU card). Using these CPU cards, a variety of multiprocessor system configurations can be implemented on the STD BUS.

Bus arbitration is done entirely in hardware, making the arbitration process transparent to software on any of the multimaster CPU cards. Wait states are automatically inserted when the 7864 tries to access global (off-card) memory or I/O while the bus is being used by another multimaster or during the actual time required for bus arbitration. A multimaster always relinquishes the bus at the end of any machine cycle during which another multimaster has requested the bus unless it has "locked" the bus with either software (8088 lock instruction prefix) or hardware (onboard lock control port). The STD BUS priority chain (PCI/PCO) is used to resolve and prioritize simultaneous bus access requests from more than one multimaster CPU card.

The 7864 features a buffered and fully expandable 8088 microprocessor operated at 4.9152 MHz in the maximum mode. The optional 8087 math coprocessor greatly simplifies and speeds up arithmetic calculations, while for software purposes it can be treated as an extension of the 8088's registers and instruction set.

The two memory sockets conform to the JEDEC 28-pin standard and either accepts 8K, 16K, 32K, or 64K ROMs or 8K byte-wide RAMs. Eight mapping options are provided for each socket. Usually one socket is mapped at the high end of the one megabyte 8088 memory map to include the 8088's power-on restart address, while the other socket is mapped at the low end to support the 8088 interrupt structure. This onboard memory is available exclusively to the 8088 CPU on the 7864; it cannot be accessed by other multimasters in the system.

The 7864 has two SBX connectors, allowing the user to add specialized I/O functions to the CPU card as required for individual applications. The SBX connector is a standard interface for I/O modules, which are available for a wide variety of I/O functions including A/D and D/A converters, serial communications, and parallel I/O.

An 8259A interrupt controller is provided to supply interrupt vectors to the 8088 for fast response to various interrupting conditions. Unique vectors can be provided for interrupts from both on-card devices (the 8087, the SBX I/O modules, and the 8253-5 counter/timer) and the STD BUS Interrupt Request signal (INTRQ*). The 8259A supports a variety of interrupt priority schemes and nesting modes.

The 8253-5 counter/timer is used in conjunction with the interrupt controller to provide periodic CPU interrupts. This feature can be useful in setting up a bus protocol for a multimaster system. The interrupt can be used to time-out the lock signal, or to determine the frequency of bus access. The 8253-5 can also supply a programmable clock output and a counter input for the SBX I/O modules.

FEATURES

- 8088 CPU with optional 8087 math coprocessor
- Multimaster capability (up to 16 CPU cards on one STD backplane)
- Up to 128K bytes of onboard ROM
- Up to 16K bytes of onboard RAM (8K by 8 devices)
- Up to 64K bytes of onboard RAM (32k by 8 devices*)
- Direct addressing of 1M byte of memory, 56K off-card I/O ports
- Two SBX connectors for user-supplied I/O modules
- 8259A interrupt controller for vectored interrupts
- 8253-5 counter/timer for periodic interrupts and SBX module clock and counter functions.
- Precision power-on and pushbutton reset circuitry

*Not available at publication. See page 2-8.

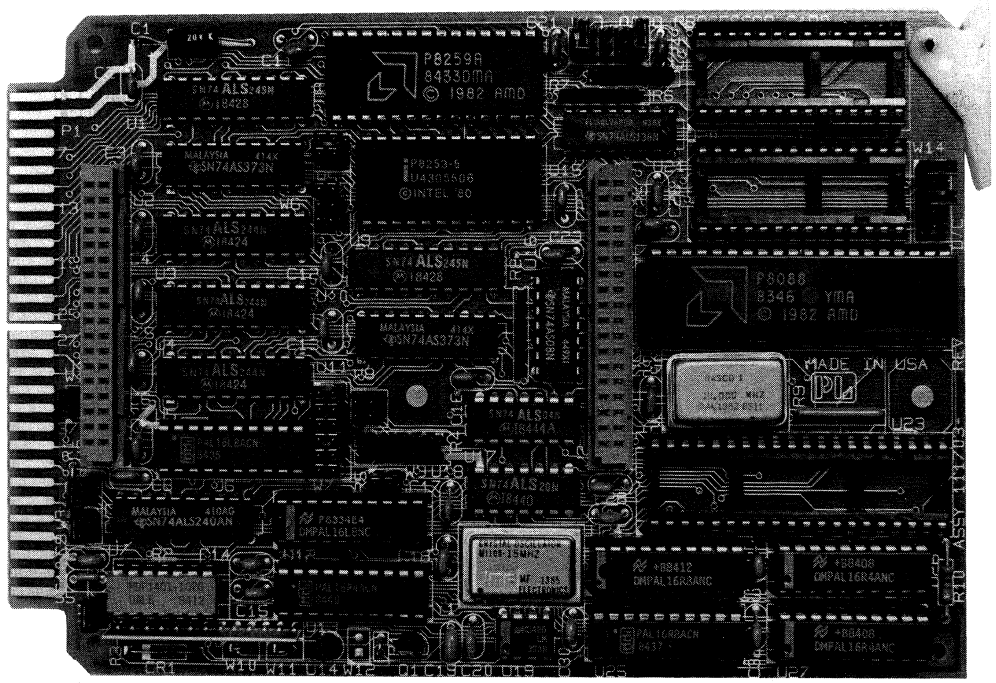


Figure 1-1. 7864 Multimaster 8088 CPU/SBX Card

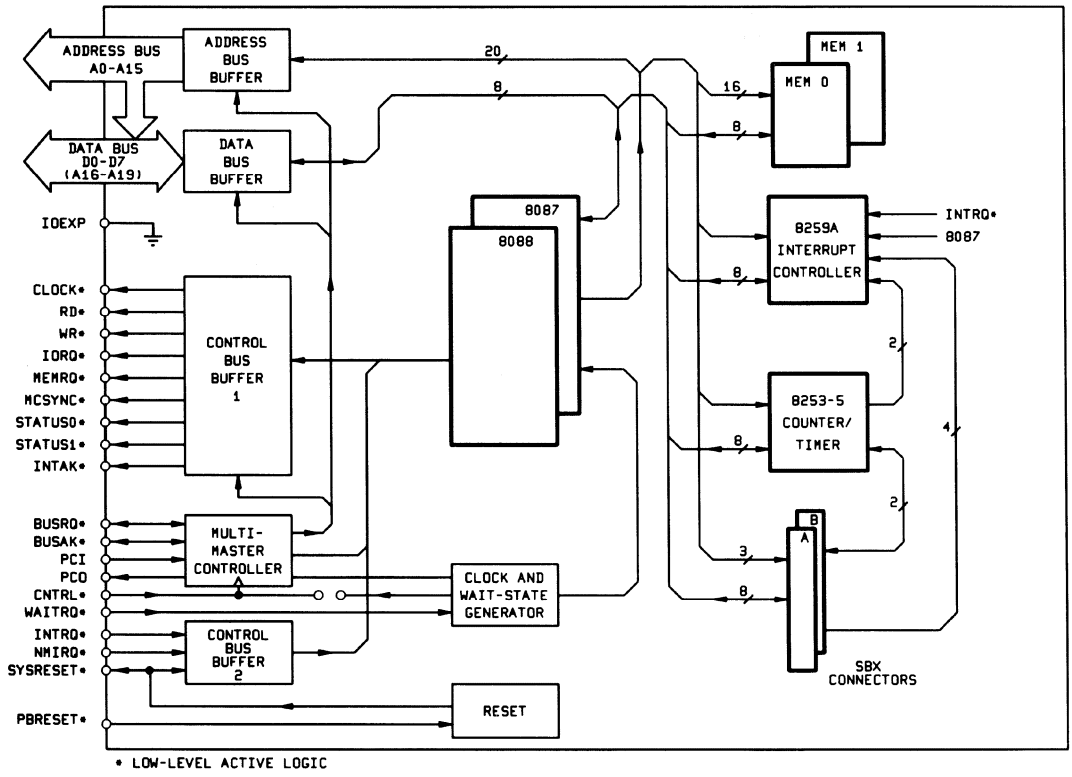


Figure 1-2. Block Diagram

FUNCTIONAL DESCRIPTION

This description defines each block in the diagram (Figure 1-2). The description and the block diagram are intended to familiarize the user with both the 7864 card and the terminology used throughout this manual.

Address Bus Buffer

This buffer provides for buffering and 3-state control of the STD address bus. Address lines A0-A15 are latched, while address lines A16-A19 are time multiplexed onto data bus lines D0-D3. (The rising edge of MCSYNC* is used by external memory cards to latch these upper address lines.) The Address Bus Buffer is 3-stated by the bus arbiter when another multimaster CPU card in the system is using the bus.

Data Bus Buffer

The Data Bus Buffer provides 3-state control, direction control, and buffering of the STD data bus (D0-D7). As noted above, the lower four data lines are time multiplexed with the upper four address lines. Like the address bus buffer, the Data Bus Buffer is controlled by the bus arbiter.

Control Bus Buffer 1

This buffer provides buffering and 3-state control of memory, I/O, and peripheral control signals. This buffer is also controlled by the bus arbiter.

Control Bus Buffer 2

This buffer is not controlled by the bus arbiter; it provides buffering for control signal inputs.

Bus Arbiter

The arbiter, implemented as a set of programmable array logic devices (PALs), allows the use of the 7864 as a multimaster CPU with other multimasters installed in the same STD backplane. When the 7864 8088 CPU attempts an off-card memory of I/O operation, the bus arbiter allows the 7864 access to the STD BUS and resolves simultaneous bus access requirements from other multimasters.

8088/8087

This 16-bit microprocessor (8-bit external data bus) and associated math coprocessor can be considered for software purposes as one CPU with greatly increased arithmetic capabilities.

Clock and Wait-State Generator

This device generates the 4.9152 MHz clock signal for the 8088 and inserts wait states when required (by controlling the 8088 READY input). Wait states are inserted when a bus access is attempted and another multimaster is currently using the bus (and during the subsequent bus arbitration cycle), during any I/O operation, and (if the 7864 has control of the STD BUS) when the STD BUS signal WAITRQ* is active. The Clock/Wait-State Generator on one multimaster CPU card in a system also provides the clock (CNTRL* on the STD BUS) used to synchronize the bus arbiters on all multimasters.

Reset

Reset provides a signal that places the card in a reset state during power-up, pushbutton reset, or DC power fail (i.e., when Vcc on-card drops below 4.65V). Precision voltage-sensing circuitry ensures that the card is held in the reset state during power-up until 60 milliseconds after Vcc reaches 4.75 minimum. The 7864 both drives and responds to SYSRESET* on the STD BUS.

MEM 1

This 28-pin JEDEC standard socket is for user-supplied memory devices (8K, 16K, 32K, or 64K ROMs or 8K RAM). The highest address in the device installed will normally be FFFFF hex. The socket can also be disabled (removed from the memory map) if required. See Figure 1-3 for memory mapping options.

MEM 0

This socket is the same as MEM 1, except that the lowest address in the device installed will normally be 00000 hex. See Figure 1-3 for memory mapping options.

Interrupt Controller (8259A).

The 8259A prioritizes and generates 8088 interrupt vectors for both onboard and STD BUS interrupts. See Figure 1-4 for onboard I/O mapping.

Counter/Timer (8253-5)

This device can provide periodic interrupts to the 8088 and provides clock and counter functions for SBX I/O modules. See Figure 1-4 for onboard I/O mapping.

SBX Connectors

These connectors allow installation of two user-supplied, 8-bit, single-width I/O expansion modules. See Figure 1-4 for onboard I/O mapping.

OPTIONS*	MEMORY SOCKET 0	MEMORY SOCKET 1
OPTION 0 (AS SHIPPED)	64Kx8 00000-0FFFF	64Kx8 F0000-FFFFF
OPTION 1	32Kx8 00000-07FFF	32Kx8 F8000-FFFFF
OPTION 2	16Kx8 00000-03FFF	16Kx8 FC000-FFFFF
OPTION 3	8Kx8 00000-01FFF	8Kx8 FE000-FFFFF
OPTION 4	64Kx8 E0000-EFFFF	64Kx8 10000-1FFFF
OPTION 5	32Kx8 F0000-F7FFF	32Kx8 08000-0FFFF
OPTION 6	8Kx8 FC000-FDFFF	8Kx8 02000-03FFF
OPTION 7	SOCKET DISABLED	SOCKET DISABLED

*Options can be independently selected for each socket

Figure 1-3. Onboard Memory Mapping Options

I/O PORT ADDRESS	OUTPUT FUNCTION	INPUT FUNCTION
0000-DFFF	(Off-card I/O)	
E000-FFBF	DO NOT USE*	
FFC0-FFCF	Reserved for SBX Connector A	
FFD0-FFDF	Reserved for SBX Connector B	
FFE0-FFE7	DO NOT USE*	
FFE8	8253-5 Counter/Timer Load Counter 0	8253-5 Read Counter 0
FFE9	8253-5 Load Counter 1	8253-5 Read Counter 1
FFEA	8253-5 Load Counter 2	8253-5 Read Counter 2
FFEB	8253-5 Control Word Register	(NOT USED)
FFEC-FFEF	DO NOT USE*	
FFF0	8259A Interrupt Controller Command/ Control Register	8259A IRR/ISR Status Register
FFF1	8259A Command/ Control Register	8259A IMR Status Registers
FFF2-FFFE	DO NOT USE*	
FFFF	Bus Lock Control	(NOT USED)

*Due to I/O Decoding, no off-card I/O can be mapped in this address block.

Figure 1-4. I/O Mapping, 7864

SPECIFICATIONS

Electrical and Environmental Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Specified)

- Supply Voltage, Vcc: 0 to 7 volts
- Auxiliary Supply Voltage, AUX V+: 0 to 15 volts
- Auxiliary Supply Voltage, AUX V-: 0 to -15 volts
- Operating Free-Air Temperature Range: 0°C to +65°C
- Storage Temperature Range: -40°C to +85°C
- Noncondensing Relative Humidity: 5% to 95%

OPERATING CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage, Vcc	4.75	5.00	5.25	Volt
Supply Voltage, AUX V+*	11.40	12.00	12.60	Volt
Supply Voltage, AUX V-*	-11.40	-12.00	-12.60	Volt
Operating Free-Air Temperature	0	25	65	°C
Noncondensing Relative Humidity	5	—	95	%

*Needed only for user-supplied SBX modules.

Electrical Characteristics

Over Operating Free-Air Temperature Range (Unless Otherwise Specified)

Parameter	Test Conditions	MIN	TYP	MAX	UNITS
I_{CC} (V_{CC})	7864, no onboard memory	—	1.4*	2.0*	A
	7864, no onboard memory, 8087 installed	—	1.7*	2.5*	A
I_{AUX+} (AUX V+)		—		0*	mA
I_{AUX-} (AUX V-)		—		0*	mA

*Plus current requirements of user-supplied SBX modules (see *SBX Interface*).

V_{CC} TRIGGERED RESET	MIN	TYP	MAX	UNITS
W5 shorting connector installed:				
V_{CC}, reset delay start (power up)	4.75	—	4.90	V
V_{CC}, SYSRESET* low (power down)	4.55	—	4.70	V
W5 shorting connector removed:				
V_{CC}, reset delay start (power up)	4.60	—	4.75	V
V_{CC}, SYSRESET* low (power down)	4.40	—	4.55	V
Hysteresis	—	200	—	mV
Delay, Reset off to SYSRESET* high	60	—	100	ms

All logic signal levels related to the 7864 that appear on the STD BUS conform to TTL requirements specified in the general *STD Series 7000 and 70C00 Specification,* Pro-Log document number 111684. See Figure 1-5, the 7864 Edge Connector Pin List, for bus input loading and output drive.

7864 MTBF (calculated using component standard failure rates specified in *Failure Rates and MTBF Calculation,* Pro-Log document number 111443) is over 20 years.

Clock Specification

- ***Nominal Frequency:*** 4.9152 MHz
- ***Frequency Stability:*** ±.01%*

*Includes initial tolerance and aging.

SBX Interface

Connectors J1 and J2 and the signals at these connectors meet all electrical specifications of the proposed IEEE P959 I/O Bus Specification, except that the maximum power supply current available to I/O modules installed in each connector is as follows:

VOLTAGE	MAXIMUM CURRENT	UNITS
+5.00V	1.0	A
+12.0V	250	mA
-12.0V	250	mA

See the SBX connector pin lists, Figures 1-6 and 1-7, for signal input loading and output drive.

SBX Bus Compliance: D8/8. User-supplied I/O modules must be 8-bit, single width. Interlocked operation is supported (the 7864 responds to wait-state requests from SBX boards); DMA operations to or from SBX boards are not supported.

Mechanical Specifications

The 7864 meets all general mechanical specifications as given in the general *STD Series 7000 and 70C00 Specification,* Pro-Log document number 111684.

Card Spacing

Requires one .5-inch center card slot (without user-supplied SBX modules).

SBX Interface

Connectors J1 and J2 meet all mechanical specifications of the proposed IEEE P959 I/O Bus Specification.

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)		
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3/A19
D6	1	55	10	9	55	1	D2/A18
D5	1	55	12	11	55	1	D1/A17
D4	1	55	14	13	55	1	D0/A16
A15		55	16	15	55		A7
A14		55	18	17	55		A6
A13		55	20	19	55		A5
A12		55	22	21	55		A4
A11		55	24	23	55		A3
A10		55	26	25	55		A2
A9		55	28	27	55		A1
A8		55	30	29	55		A0
RD* (1)		55	32	31	55		WR* (1)
MEMRQ* (1)		55	34	33	55		IORQ* (1)
MEMEX			36	35	(4)		IOEXP
MCSYNC* (1)		55	38	37			REFRESH*
STATUS 0* (1)		55	40	39	55		STATUS 1* (1)
BUSRQ* (1)	1	55	42	41	55	1	BUSAK* (1)
INTRQ* (1)	1		44	43	55		INTAK* (1)
NMIRQ* (1)	1		46	45		1 (2)	WAITRQ*
PBRESET*	(3)		48	47	220		SYSRESET*
CNTRL*	1	55	50	49	55		CLOCK* (1)
PCI	3		52	51	18		PCO
AUX GND			54	53			AUX GND
AUX -V	IN		56	55		IN	AUX +V

* Low-level active logic
One LSTTL Load = -0.4 mA

(1) Drive and loading shown are with resistor pack R2 removed. R2 is installed on one multimaster per system; for that card, add 10 TTL loads to input load and subtract 10 TTL loads from output drive.

(2) Add 21 TTL loads if R2 is installed (see note 1).

(3) Switch input

(4) Can be jumpered to ground.

Figure 1-5. STD Edge Connector

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
-12V		OUT	2	1	OUT		+12V
+5V		OUT	4	3			GND
MCLK		18	6	5	25		RESET
			8	7	55		LA2 (MA2)[1]
			10	9	55		LA1 (MA1)
IR6 (MINTR 1)	1		12	11	55		LA0 (MA0)
IR5 (MINTR 0)	1		14	13	9		PWR* (IOWRT*)
MWAITB* (MWAIT*)	1		16	15	9		PRD* (IORD*)
+5V		OUT	18	17			GND
CS3* (MCS 1*)		18	20	19	25	1	D7 (MD7)
CS2* (MCS 0*)		18	22	21	25	1	D6 (MD6)
			24	23	25	1	D5 (MD5)
			26	25	25	1	D4 (MD4)
OPT1 B (OPT 1)		5	28	27	25	1	D3 (MD3)
OPT0 B (OPT 0)	1		30	29	25	1	D2 (MD2)
			32	31	25	1	D1 (MD1)
			34	33	25	1	D0 (MD0)
+5V		OUT	36	35			GND

[1] Parentheses indicate SBX mnemonic if different from 7864 signal name
One LSTTL load = -0.4 mA

Figure 1-6. Pin List, SBX Connector B, J2

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
-12V		OUT	2	1	OUT		+12V
+5V		OUT	4	3			GND
MCLK		18	6	5	25		RESET
			8	7	55		LA2 (MA2)[1]
			10	9	55		LA1 (MA1)
IR4 (MINTR 1)	1		12	11	55		LA0 (MA0)
IR3 (MINTR 0)	1		14	13	9		PWR* (IOWRT*)
MWAITA* (MWAIT*)	1		16	15	9		PRD* (IORD*)
+5V		OUT	18	17			GND
CS1* (MCS 1*)		18	20	19	25	1	D7 (MD7)
CS0* (MCS 0*)		18	22	21	25	1	D6 (MD6)
			24	23	25	1	D5 (MD5)
			26	25	25	1	D4 (MD4)
OPT1 A (OPT 1)		5	28	27	25	1	D3 (MD3)
OPT0 A (OPT 0)	1		30	29	25	1	D2 (MD2)
			32	31	25	1	D1 (MD1)
			34	33	25	1	D0 (MD0)
+5V		OUT	36	35			GND

[1] Parentheses indicate SBX mnemonic if different from 7864 signal name

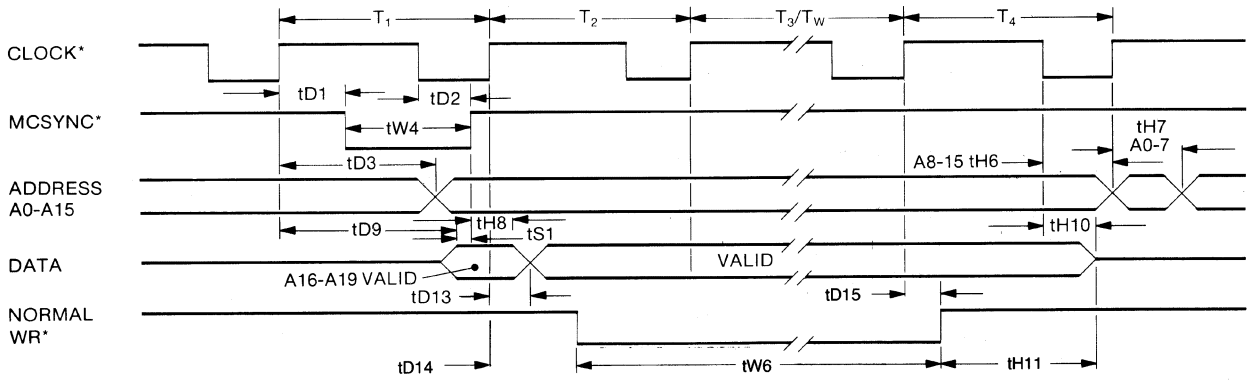
Figure 1-7. Pin List, SBX Connector A, J1

Mating connectors (not supplied with the 7864) are:

MANUFACTURER	PART NO.
T&B Ansley	609-BX366
Viking	VSP01VT18A01 or 000292-0003

Timing Specifications

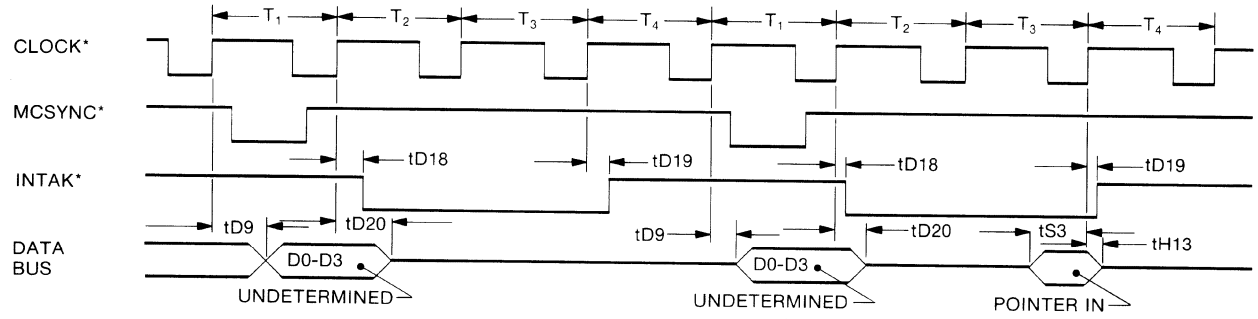
Timing for 7864 STD BUS interface signals is shown in Figures 1-8 through 1-12. The timing has been divided into six functional groups: Bus Status, Bus Read, Bus Write, Bus Interrupt, Bus Wait, and Bus Exchange Timing. All times shown have been derated to include a temperature range of 0 to +65°C, a supply range of 4.75V to 5.25V, and a 45 pF load.



SYMBOL	PARAMETER	4.9152 MHz	
		MIN	MAX
tD1	Delay from CLOCK* to MCSYNC* low	61	
tD2	Delay from CLOCK* to MCSYNC* high		102
tD3	Delay from CLOCK* to Address 0-15		125
tD9	Delay from CLOCK* to Address 16-19		125
tD13	Delay from CLOCK* to Data Valid		119
tD14	Delay from CLOCK* to Normal WR* low	48	87
tD15	Delay from CLOCK* to Normal WR* high	48	87
tH6	Address 8-I5 hold after CLOCK*	69	
tH7	Address 0-7 hold after CLOCK*	5	
tH8	Address 16-19 hold after MCSYNC*	53	
tH10	Data hold after CLOCK*	10	
tH11	Data hold after normal WR*	60	
tS1	Address 16-19 setup to MCSYNC*	64	
tW4	MCSYNC* pulse width	67	
tW6	Normal WR* pulse width	406	

All times given in nanoseconds.

Figure 1-10. Bus Write Timing

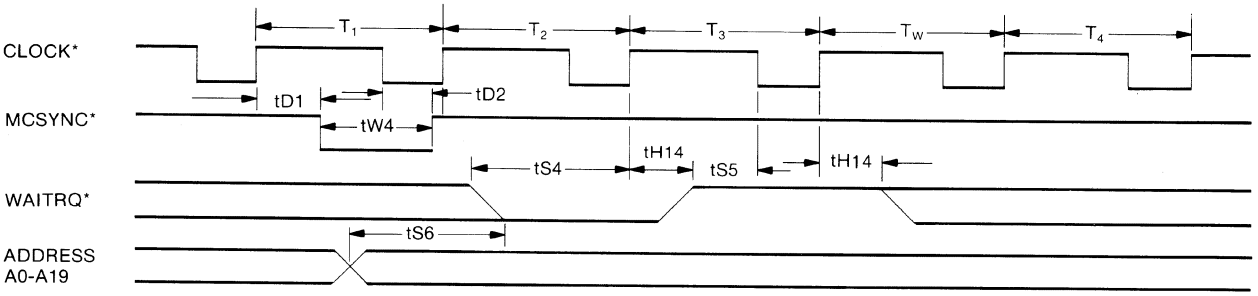


SYMBOL	PARAMETER	4.9152 MHz	
		MIN	MAX
tD9	Delay from CLOCK* to Address 16-19		125
tD18	Delay from CLOCK* to INTAK* low	116	155
tD19	Delay from CLOCK* to INTAK* high	48	87
tD20	Delay from CLOCK* to Data Bus 3-State		51
tH13	Interrupt vector hold from CLOCK*	6	
tS3	Interrupt vector setup to CLOCK*	52	

All times given in nanoseconds.

NOTE: The illustrated example does not show possible additional clock cycles between T4 of first cycle and T1 of second INTAK cycle. These clock cycles occur if the 8088 internal queue is not full. These clock cycles do not affect system operation, only total interrupt response time.

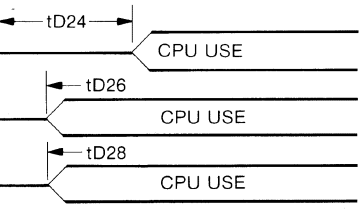
Figure 1-11. Bus Interrupt Timing



SYMBOL	PARAMETER	4.9152 MHz	
		MIN	MAX
tDI	Delay from CLOCK* to MCSYNC* low	61	
tD2	Delay from CLOCK* to MCSYNC* high		102
tH14	WAITRQ* hold after CLOCK*	9	
tS4	WAITRQ* low setup to CLOCK*	26	
tS5	WAITRQ* high setup to WAITRQ*	26	
tS6	Address 0-19 setup to WAITRQ*	256	
tW4	MCSYNC* pulse width	67	

All times given in nanoseconds.

Figure 1-12. Bus Wait Request Timing



4.9152 MHz	
MIN	MAX
63	
288	
88	
212	
49	
283	

Section 2
INSTALLATION

In selecting a power supply for an STD BUS system that uses one or more 7864 cards, make sure that all electrical requirements of the 7864 as specified in Section 1 (Electrical Specifications) are met. Each 7864 can draw more than 2.5 amps of current from the 5V supply (Vcc) with memory installed. The power supply selected, the power distribution cables and connectors, and the STD BUS backplane must be able to supply the required current to each card while maintaining Vcc within the ±5% tolerance specified.

As shipped, the 7864 is held in a reset state until 60 milliseconds after Vcc reaches 4.75V minimum during power-up, ensuring that the card is operated within specifications. Due to component tolerances in the reset circuitry, the actual level at which reset is released and operation begins may be as high as 4.90V. Voltage drops in cabling, connectors, and the STD BUS backplane may require that the power supply be adjusted before reset is released. See the following information on Reset, Jumper W5, for more information.

PHYSICAL INSTALLATION

The 7864 operates as part of an STD BUS system. A 7864 can be inserted into any slot in the STD BUS card rack, although multimaster systems require certain physical arrangements of cards in the card rack. These arrangements are discussed in detail under "Priority Chain." When installed, the card ejector tab must be at the top as shown in Figure 2-1. If access to the card is needed for testing or servicing, a card extender such as the Pro-Log 7901 can be used. Card extenders tend to degrade STD BUS signals, which may cause problems with dynamic RAM or other STD cards with stringent bus timing or noise requirements. The use of more than one or two extenders may cause problems in any system.

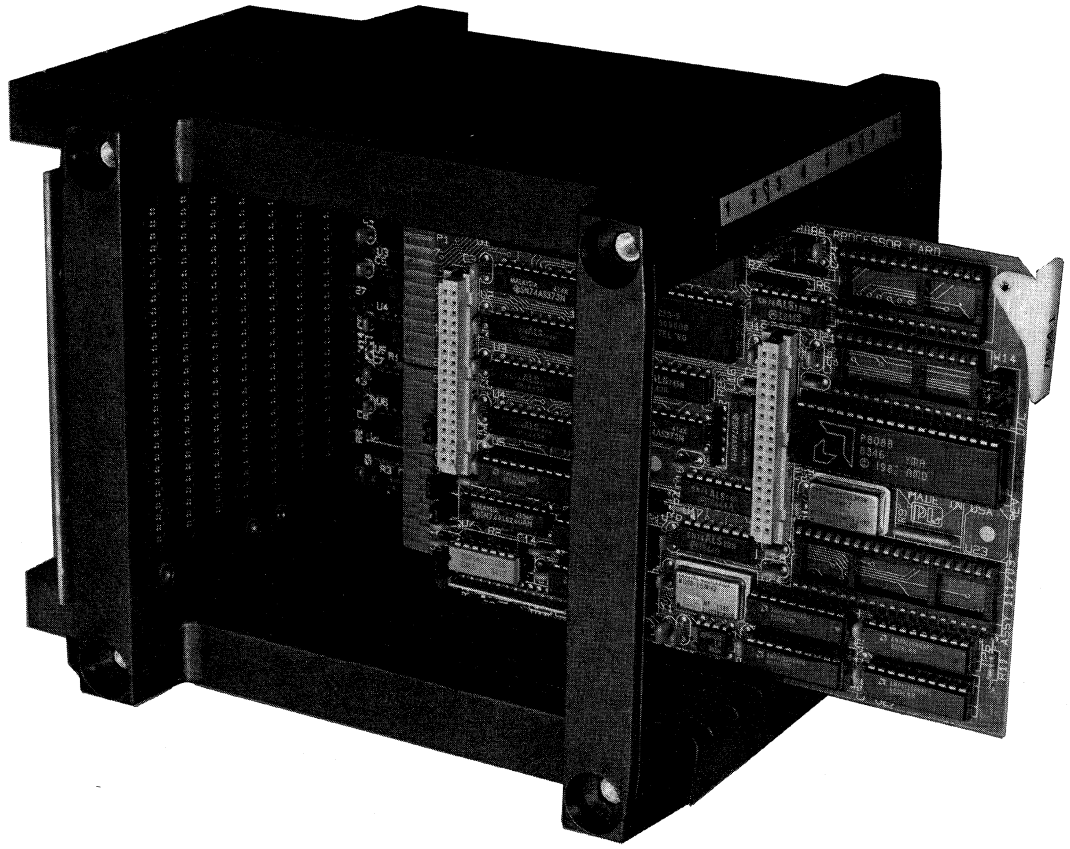


Figure 2-1. Installation

Priority Chain

Since the priority chain lines on the STD BUS (PCO, pin 51, and PCI, pin 52) are used for bus arbitration in a multimaster system, multiple 7864 and/or other multimaster CPU cards must be installed in the card rack so the priority chain is continuous between them, i.e., PCO of one multimaster drives PCI of the next. Multimaster CPU cards are usually installed in adjacent slots in the card rack. This is not possible if SBX modules are installed on a 7864 since the added height of the modules requires an extra card slot. The PCI-PCO Jumper Board which is shipped with the 7864 must be inserted in the card slot occupied by the SBX modules to maintain continuity of the priority chain (see Figure 2-2a). If a non-multimaster card (such as a memory or I/O card) must be installed between two multimasters, it must not use the priority chain on-card but must pass the chain through by connecting PCI to PCO onboard (see Figure 2-2b).

The PCI input to the rightmost multimaster in the STD card rack should never be driven, since the rightmost multimaster has the highest priority of all multimasters in the system. Usually this is accomplished by installing the multimaster CPU cards starting with the rightmost slot in the card rack (see Figure 2-2a, b, and d). If this cannot be done, it is necessary to leave the card slot immediately to the right of the rightmost multimaster vacant (see Figure 2-2c) if any card to the right of the multimasters drives or uses the priority chain.

STD BUS cards that use the priority chain for another purpose (such as I/O cards that use the chain for interrupt prioritization) can be used in the same card rack with 7864 or other multimaster CPU cards. To do this, the priority chain must be broken, either by leaving a vacant card slot between the multimasters and the other cards (see Figure 2-2c) or by removing the shorting connector from a jumper (W4 on the 7864) so the PCO output of the lowest-priority (leftmost) multimaster is not driven (see Figure 2-2d). If the lowest priority 7864 has SBX modules installed, the PCI-PCO Jumper Board can be omitted (Figure 2-2d). The system then has two separate priority chains with cards using each in separate sections of the card rack.

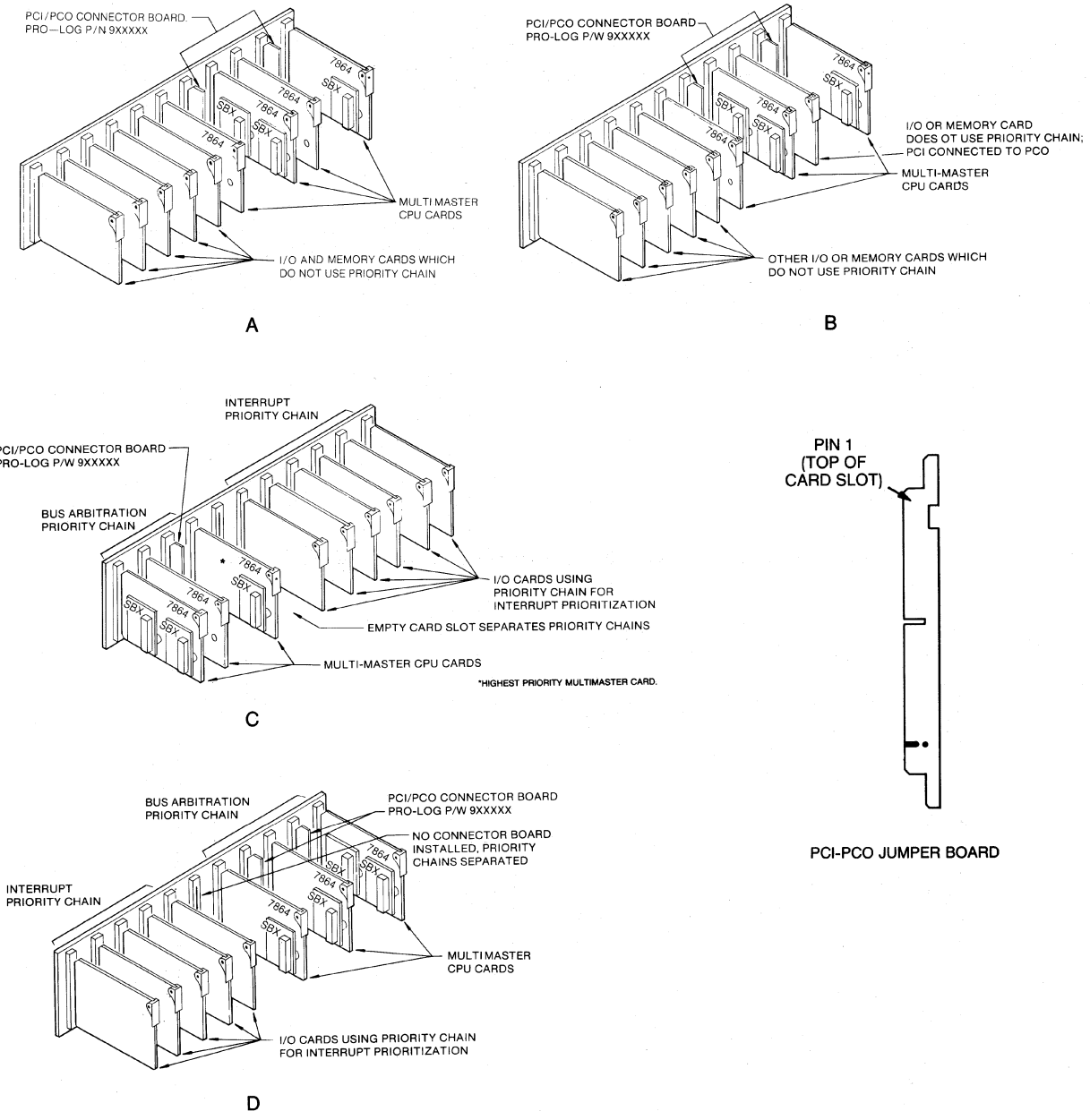


Figure 2-2. Multimaster Installation Options

CARD LAYOUT AND JUMPERS

The 7864 has onboard jumpers to configure the card to meet system requirements. The jumper configurations consist of unshrouded headers and shorting connectors as shown in Figure 2-3. The shorting connectors can be removed and installed without the use of soldering equipment. Figure 2-4 lists sources for the shorting connectors.

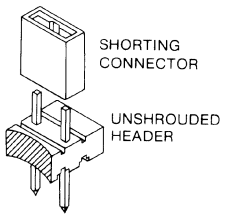
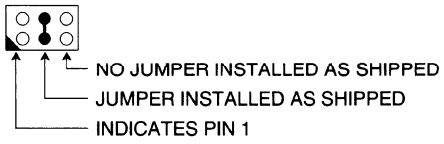


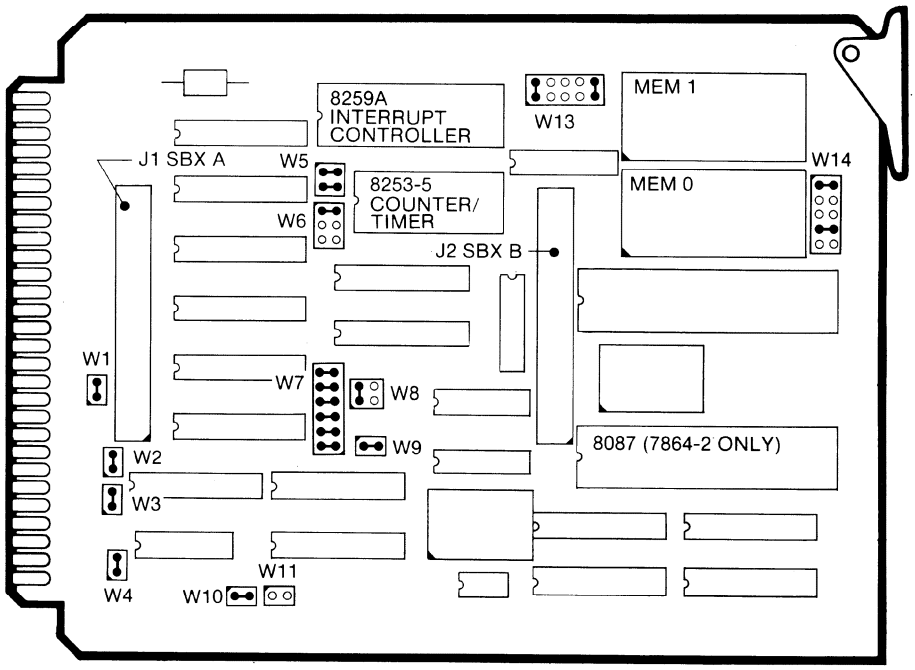
Figure 2-3. Jumper Configuration

SOURCE	PART NUMBER
Pro-Log	902520
Elco	008261024200870
Amp	531220-3

Figure 2-4. Sources for Shorting Connector

Figure 2-5 on the following pages provides a reference for the location and a brief description of each jumper on the 7864. The discussion following Figure 2-5 divides the jumper options into five functional groups: Multimaster Configuration, Reset, Memory and I/O, Interrupt, and SBX Connectors.





JUMPER GROUP	JUMPER INSTALLED	JUMPER REMOVED	DESCRIPTION	AS SHIPPED	SEE PAGE
W1	1-2 —	— 1-2	IOEXP DRIVE ENABLE • IOEXP grounded • IOEXP driven by another card	*	2-9
W2	1-2 —	— 1-2	BUS INTRQ* ENABLE • Enable • Disable	*	2-9

Figure 2-5. Physical Layout and Jumper Options

JUMPER GROUP	JUMPER INSTALLED	JUMPER REMOVED	DESCRIPTION	AS SHIPPED	SEE PAGE
W3			CNTRL* SOURCE SELECT		
	1-2	—	• Driven by on-card clock generator	*	2-6
	—	1-2	• Driven by external source		
W4			PCO DRIVE ENABLE		
	1-2	—	• PCO driven	*	2-7
	—	1-2	• PCO not driven		
W5			COUNTER/TIMER OUT1/OPT 1		
	3-4	1-2	• OUT 1 drives OPT 1, SBX A		2-10
	1-2	3-4	• OUT 1 drives OPT 1, SBX B		
	1-2, 3-4	—	• OUT 1 drives OPT 1, both A&B	*	
W6			OPT0/COUNTER/TIMER CLK 2 SOURCE		
	5-6	3-4, 1-2	• CLK 2 input is OPT 0, SBX A		2-10
	3-4	5-6, 1-2	• CLK 2 input is OPT 0, SBX B		2-10
	1-2	3-4, 5-6	• CLK 2 input is 1.2288 MHz	*	
W7			MEMORY MAPPING		
			MEM 0: (W7, Pins 1-2, 3-4, 5-6)		
	1-2, 3-4, 5-6	—	• 00000-0FFFF (64K)	*	
	1-2, 3-4	5-6	• 00000-07FFF (32K)		
	1-2, 5-6	3-4	• 00000-03FFF (16K)		
	1-2	3-4, 5-6	• 00000-01FFF (8K)		
	3-4, 5-6	1-2	• E0000-EFFFF (64K)		
	3-4	1-2, 5-6	• F0000-F7FFF (32K)		
	5-6	1-2, 3-4	• FC000-FDFFF (8K)		
	—	1-2, 3-4, 5-6	• SOCKET DISABLED		2-8
			MEM 1: (W7, Pins 7-8, 9-10, 11-12)		
	7-8, 9-10, 11-12	—	• F0000-FFFFF (64K)	*	
	7-8, 9-10	11-12	• F8000-FFFFF (32K)		
	7-8, 11-12	9-10	• FC000-FFFFF (16K)		
	7-8	9-10, 11-12	• FE000-FFFFF (8K)		
	9-10, 11-12	7-8	• 10000-1FFFF (64K)		
	9-10	7-8, 11-12	• 08000-0FFFF (32K)		
	11-12	7-8, 9-10	• 02000-03FFF (8K)		
	—	7-8, 9-10, 11-12	• SOCKET DISABLED		
W8			LOCK MODE SELECT		
	1-2	3-4	• DMA lock enable	*	
	1-3	2-4	• Hardware lock enable		2-7
	2-4	1-3	• Lock always asserted (single CPU system)		
	—	1-2, 3-4	• Software Lock only		
W9			INTRQ* VECTOR SOURCE SELECT		
	1-2	—	• Bus vector during INTAK*	*	2-10
	—	1-2	• SCC provides vector during INTAK*		
W10			RESET VOLTAGE SELECT		
	1-2	—	• Power-on reset level 4.75V min.	*	2-7
	—	1-2	• Power-on reset level 4.75V max.		
W11			PRO-LOG USE ONLY		
W13			MEM 1 CONFIGURATION		
	3-4, 5-6, 7-8	1-2, 9-10	• 8K ROM		
	1-2, 9-10	3-4, 5-6, 7-8	• 16K ROM	*	2-8
	1-2, 3-4, 9-10	5-6, 7-8	• 32K ROM		
	3-4, 5-6, 9-10	1-2, 7-8	• 64K ROM		
	1-2, 7-8	3-4, 5-6, 9-10	• 8K RAM		
	4-6, 7-8, 9-10	1-2, 3-5	• 32K RAM		
W14			MEM 0 CONFIGURATION		
	3-4, 5-6, 7-8	1-2, 9-10	• 8K ROM		
	1-2, 9-10	3-4, 5-6, 7-8	• 16K ROM		
	1-2, 3-4, 9-10	5-6, 7-8	• 32K ROM		
	3-4, 5-6, 9-10	1-2, 7-8	• 64K ROM		
	1-2, 7-8	3-4, 5-6, 9-10	• 8K RAM	*	2-8
	4-6, 7-8, 9-10	1-2, 3-5	• 32K RAM		

Figure 2-5 (Continued)

Multimaster Configuration

Jumpers W3, W4, and W8 and Resistor Pack R2 affect the operation of the 7864 with other multimaster CPU cards in an STD BUS system. They must be configured correctly to ensure proper operation of the bus arbitration logic. Figure 2-6 shows how these jumpers should be configured on each 7864 card in a multimaster system or on a 7864 used in a single-CPU system. Figures 2-7 through 2-9 and their respective discussions describe these jumpers individually.

Resistor Pack R2, Control Pull-ups (Figure 2-6)

Resistor pack R2 contains 1000-ohm pull-up resistors which are required on certain STD BUS control signals (INTRQ*, NMIRQ*, WAITRQ*, INTAK*, RD*, WR*, MEMRQ*, CLK*, MCSYNC*, BUSRQ*, and BUSAK*) in a multimaster system. This resistor pack should be installed on one multimaster card in a card rack. The resistor pack containing these pull-up resistors should be removed from all other multimasters to prevent excessive loading of these control signals.

7864 #	DESCRIPTION	JUMPER W3	JUMPER W4	JUMPER W8		RESISTOR PACK R2
MULTIPLE CPU SYSTEM:						
1	Highest priority (rightmost in rack)	1-2*	1-2	1-2	DMA lock mode or	INSTALLED
				1-3	hardware lock mode or	
				NONE	software lock only	
2 ↕ n-1		NONE	1-2	1-3	Hardware lock mode or	REMOVED
				NONE	software lock only	
n (2-16)	Lowest priority (Leftmost in rack)	NONE	NONE	1-3	Hardware lock mode or	REMOVED
				NONE	software lock only	
SINGLE CPU SYSTEM:						
1		1-2	NONE	2-4	DMA lock always asserted	INSTALLED

*Jumper pins with shorting connectors installed

Figure 2-6. Multimaster Configuration Jumpers

CNTRL Source Select, Jumper W3 (Figure 2-7)*

This jumper selects whether the clock (CNTRL*, Pin 50 on the STD BUS) used by all multimaster CPU cards in the system for bus arbiter synchronization is provided by this card or by another multimaster. Only one multimaster in the system can drive CNTRL* and it should be the highest priority multimaster in the system (the rightmost multimaster installed in the card rack). If the 7864 is to be the highest priority multimaster or is to be used as the only CPU card in the system, a shorting connector should be installed in Jumper W3; if not, the shorting connector should be removed.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
This card drives CNTRL*	1-2**
Another multimaster drives CNTRL*	NONE

**As shipped

Figure 2-7. CNTRL* Source Select, Jumper W3

PCO Drive Enable, Jumper W4 (Figure 2-8)

This jumper determines whether the priority chain output (PCO, Pin 51 on the STD BUS) is driven by the 7864 bus arbiter or left floating. When a shorting connector is installed in W4, PCO is driven. For proper bus arbitration, all 7864 cards in a multimaster STD system must have this jumper installed unless the 7864 is the lowest priority multimaster (the leftmost multimaster installed in the card rack). The shorting connector must be removed from Jumper W4 on this card if peripheral or memory cards installed to the left of this lowest priority multimaster use the priority chain for some other purpose (such as interrupt prioritization). If SBX modules are installed on this leftmost 7864, the priority chain can also be broken by not installing the PCI-PCO Connector Board in the STD BUS card slot occupied by the SBX modules.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
PCO is driven by this card	1-2**
PCO is not driven	NONE

**As shipped

Figure 2-8. PCO Drive Enable, Jumper W4

Lock Mode Select, Jumper W8 (Figure 2-9):

The 7864 has an onboard one-bit output port (mapped as port FFFF, bit D0) that can be set to lock the bus, i.e., to prevent any other multimaster from taking control of the STD BUS away from the 7864 until the port has been cleared. Jumper W8 enables this bus lock function and determines whether Hardware Lock Mode or DMA Lock Mode is active when the output port bit has been set.

If no shorting connector is installed in Jumper W8, the lock control port is disabled. If a shorting connector is installed in W8 pins 1-3, Hardware Lock will be active when the output port bit is set. Any number of 7864s or other multimasters in a system can each implement this bus lock mode.

If a shorting connector is installed in W8 pins 1-2, DMA Lock Mode is active when the output port bit is set. This lock mode can only be used by the highest priority multimaster in the system (the rightmost multimaster installed in the card rack). When DMA Lock Mode is selected, no other multimaster can gain access to the bus, as with Hardware Lock Mode. In addition, BUSRQ* and BUSAK* on the STD BUS are no longer used for bus arbitration but are available for use by DMA controllers in normal BUSRQ*/BUSAK* operation. Bus access requests from all other multimasters are inhibited by disabling the STD BUS priority chain so only the highest priority multimaster can implement this mode. DMA operations in a multimaster STD system are only possible when the DMA Lock Mode is active.

In a single CPU system, it may be desirable to permanently select the DMA Lock Mode since bus arbitration will never be required, and normal DMA operations will be supported; DMA Lock Mode is always active when a shorting connector is inserted in Jumper W8, pins 2-4.

In addition to these bus lock modes, a software lock mode is always available. In this mode, a 7864 Multimaster CPU can retain control of the bus for the duration of a multicycle instruction, through the use of a lock prefix to the instruction in the program being executed.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
DMA lock is enabled	1-2
Hardware lock is enabled	1-3**
DMA lock is always asserted	2-4
Hardware and DMA lock disabled: software lock only	NONE

*As shipped

Figure 2-9. Lock Mode Select Jumper W8

Reset, Jumper W10 (Figure 2-10)

This jumper sets the voltage level to which Vcc on-card must rise before reset (and SYSRESET* on the STD BUS) is released, after a time delay. As shipped, with a shorting connector installed in Jumper W10 pins 1-2, Vcc must reach +4.75V minimum. This ensures that all devices on the 7864 are operating within specification (Vcc = 5V ± 5%) when reset is released. Due to component tolerances, the actual voltage level at which reset is released may be as high as 4.90V. Because of voltage drops in cabling and in the STD BUS backplane and card edge connectors, Vcc on the card may never rise above 4.90V and the card will not come out of the reset state. Adjustment of the power supply or remote sensing of Vcc on the backplane may be required.

Removal of the shorting connector from Jumper W10 lowers the Vcc voltage level at which reset is released to 4.75V maximum, 4.60V minimum. Adjustment of the powr supply may not then be necessary. Note that if this shorting connector is removed, reset may be released before Vcc has risen above 4.75V and the card may be operated out of specification. Pro-Log recommends that you leave the W10 shorting connector in place and adjust Vcc at the power supply if necessary to ensure correct operation.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
*Power-on reset level is 4.75V minimum	1-2**
Power-on reset level is 4.75V maximum	NONE

*As shipped

Figure 2-10. Reset Voltage Select, Jumper W10

Memory and I/O

The 7864 has two memory sockets: MEM 1 and MEM 0. Jumpers W13 and W14, respectively, determine what type and size of memory device can be installed in each socket and Jumper W7 determines where each device is mapped in the 8088 CPU one-megabyte address range.

The 7864 memory sockets can accept JEDEC standard byte-wide ROMs and RAMs with an access time of 300 nanoseconds or less. Refer to Figure 2-11 for a list of recommended memory devices.

The only jumper that affects I/O is W1, which selects whether or not IOEXP, pin 35 on the STD BUS, is grounded onboard the 7864.

MEMORY TYPE	MEMORY SIZE	MANUFACTURER'S PART NUMBER	ACCESS TIME (nS)
EPROM	8K	Intel 2764	300 max
	16K	Intel 27128 AMD 27128	
	32K	Intel 27256 AMD 27256	
	64K	Intel 27512 AMD 27512	
RAM	8K	Hitachi HM6264 LP-15 Toshiba TC5565 PL-15	200 max
	32K	(1)	

(1) This device not available at publication

Figure 2-11. Recommended Memory Devices

Memory Socket Configuration, Jumpers W13 and W14 (Figure 2-12)

These jumpers select what type of device is to be installed in sockets MEM 1 and MEM 0. Each socket can be independently configured to accept 8K, 16K, 32K, or 64K ROMS or 8K RAMs. (Pro-Log believes that JEDEC-compatible 32K RAMs will also be supported when these devices become available.) Jumper W13 configures socket MEM 1 and W14 configures socket MEM 0.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
8K ROM	1-2
16K ROM	1-2, 9-10[1]
32K ROM	1-2, 3-4, 9-10
64K ROM	3-4, 5-6, 9-10
8K RAM	1-2, 7-8[2]
32K RAM[3]	4-6, 7-8

[1]As shipped, W13 (MEM 1)
[2]As shipped, W14 (MEM 0)
[3]Device not available at publication

Figure 2-12. Memory Socket Configuration
Jumpers W13 (MEM 1) and W14 (MEM 0)

Memory Mapping, Jumper W7 (Figure 2-13)

Jumper W7 determines the mapping of the memory devices installed in sockets MEM 1 and MEM 0. Shorting connectors installed in pins 1 through 6 determine the mapping of the device in MEM 0; those installed in pins 7 through 12 determine the mapping of the device in MEM 1. There are eight mapping options for each socket. If the socket is not to be used (no memory device is to be installed), the last option should be selected disabling the socket and removing it from the memory map.

To prevent the selection of two options that map both sockets into the same address range, certain combinations of options for the two sockets cannot be used. For example, if MEM 0 Option 5 is selected, then MEM 1 Options 0, 2, 4, and 6 cannot be used. (MEM 0 Option 5 requires that no shorting connector be installed in W7 pins 11-12, while MEM 1 Options 0, 2, 4, and 6 require the installation of this jumper.) Unusable combinations occur only when Option 5 or 6 is selected for either socket; these options require that certain shorting connectors not be installed.

For the most efficient use of memory space, the selected mapping option should use a block of memory of the same size as the device to be installed in the socket. For example, Option 2 for socket MEM 0 maps the socket at the address block 00000-03FFF hex, a 16K block of memory; a 16K memory device should be used. If an 8K device is installed, it will be redundantly addressed in the upper half of the 16K block. If a 32K device is installed, the upper 16K of the device cannot be accessed. Additionally, two options should never be selected that map both sockets into the same address block.

DESCRIPTION			PINS WITH SHORTING CONNECTORS INSTALLED	
SOCKET	OPTION	ADDRESS RANGE	PINS 1-6	PINS 7-12
MEM 0:	0	00000-0FFFF (64K BLOCK)**	1-2,3-4,5-6	
	1	00000-07FFF (32K BLOCK)	1-2,3-4	
	2	00000-03FFF (16K BLOCK)	1-2,5-6	DON'T CARE
	3	00000-01FFF (8K BLOCK)	1-2	
	4	E0000-EFFFF (64K BLOCK)	3-4,5-6	
	5	F0000-F7FFF (32K BLOCK)	3-4	(No connector in 11-12)
	6	FC000-FDFFF (8K BLOCK)	5-6	(No connector in 9-10, 11-12)
	7	SOCKET DISABLED	NONE	DON'T CARE
MEM 1:	0	F0000-FFFFF (64K BLOCK)**		7-8,9-10,11-12
	1	F8000-FFFFF (32K BLOCK)		7-8,9-10
	2	FC000-FFFFF (16K BLOCK)	DON'T CARE	7-8,11-12
	3	FE000-FFFFF (8K BLOCK)		7-8
	4	10000-1FFFF (64K BLOCK)		9-10,11-12
	5	08000-0FFFF (32K BLOCK)	(No connector in 5-6)	9-10
	6	02000-03FFF (8K BLOCK)	(No connector in 3-4, 5-6)	11-12
	7	SOCKET DISABLED	DON'T CARE	NONE

**As shipped

Figure 2-13. Onboard Memory Mapping, Jumper W7

IOEXP Drive, Jumper W1 (Figure 2-14)

If a shorting connector is installed in Jumper W1 pins 1-2, IOEXP (pin 35 on the STD BUS) is connected to ground. If the connector is removed, IOEXP is not connected on the 7864 and can be driven by some other card in the system if necessary. IOEXP is defined in the 8088 Bus Specification as an enable line (low-level active) for I/O cards that decode an 8-bit I/O address instead of the 8088's full 16-bit address.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
IOEXP grounded	1-2**
IOEXP driven by another card	NONE

**As shipped

Figure 2-14. IOEXP Drive Example, Jumper W1

Interrupt Options

Jumpers W2 and W9 determine the response of the 7864 to maskable interrupt requests from the STD BUS (INTRQ*, pin 44).

INTRQ Enable, Jumper W2 (Figure 2-15)*

If a shorting connector is installed in Jumper W2 pins 1-2, the 7864 can respond to INTRQ* on the STD BUS. If the connector is removed, the 7864 does not respond to INTRQ*. This jumper is used to select which multimasters in a system respond to STD BUS INTRQ*

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
This card responds to STD BUS INTRQ*	1-2**
Does not respond to STD BUS INTRQ*	NONE

**As shipped

Figure 2-15. INTRQ* Enable, Jumper W2

INTRQ Vector Source Select, Jumper W9 (Figure 2-16)*

The 8088 CPU responds to a maskable interrupt request by executing an interrupt acknowledge cycle during which an 8-bit vector is read in on the processor data bus. This vector is normally provided by the interrupting device and is used by the processor to locate the correct interrupt service routine. If a shorting connector is installed in Jumper W9 pins 1-2, the 8088 executes an interrupt acknowledge cycle and reads a vector (which must be supplied by the interrupting device) from the STD data bus in response to an STD BUS INTRQ*. Since bus access is required to read this vector and only one multimaster can have access to the bus during the interrupt acknowledge cycle when the interrupting device places its vector on the bus, only one multimaster in the system can have this jumper installed.

When the shorting connector is removed from Jumper W9, INTRQ* can no longer directly cause an 8088 maskable interrupt. However, INTRQ* is permanently connected (through a buffer) to one of the interrupt request inputs (IR1) of the 8259A Interrupt Controller. The Interrupt Controller can generate an onboard interrupt in response to INTRQ* and provide a vector on-card when the interrupt is acknowledged. Since the source of the interrupt is on-card, access to the STD BUS is not required during the interrupt acknowledge cycle, so any or all multimasters in the system can simultaneously respond to STD BUS INTRQ* in this way.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Vector read from STD BUS during INTAK*	1-2**
Interrupt Controller provides vector during INTAK*	NONE

**As shipped

Figure 2-16. INTRQ* Vector Source Select, Jumper W9

SBX Connector Option Lines

These jumpers allow one input and one output from the counter/timer to be brought out to the SBX connectors on the SBX option lines (OPT0 and OPT1).

OPT1/Counter/Timer Channel 1 Output, Jumper W5 (Figure 2-17)

The output from channel 1 of the counter/timer can be brought out to the SBX connectors using this jumper, providing a programmable clock for SBX modules. Insertion of a shorting connector in pins 1-2 connects the output to option line 1 of SBX connector B; a shorting connector in pins 3-4 connects the output of option line 1 of SBX connector A.

Pins 2 and 4 of this jumper group also serve as the required wirewrap posts on the SBX baseboard (the 7864) which are connected to option line OPT1 on SBX connectors A and B respectively. If a user-supplied SBX module requires some other signal from the 7864, it can be wirewrapped to these pins.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Counter/Timer OUT1 drives OPT1, SBX A	3-4
Counter/Timer OUT1 drives OPT1, SBX B	1-2
Counter/Timer OUT1 drives OPT1A & OPT1B	1-2, 3-4**

**As shipped

Figure 2-17. OPT1/Counter/Timer Chan. 1 Output, Jumper W5

OPT0/Counter/Timer CLK2 Input, Jumper W6 (Figure 2-18)

This jumper selects the source for the clock input of counter/timer channel 2. If a shorting connector is inserted in pins 3-4 or 5-6, the source of the channel 2 clock is option line 0 from either SBX connector A or B respectively. This allows channel 2 of the counter/timer to serve as a counter for some SBX function.

If a shorting connector is inserted in jumper W6, pins 1-2, the clock source is the same as that of the other counter/timer channels: a 1.2288 MHz signal generated onboard the 7864.

Pins 4 and 6 of this jumper group also serve as the required SBX baseboard wirewrap posts which are connected to option line OPT0 on SBX connectors A and B respectively. If a user-supplied SBX module requires some other signal from the 7864, it can be wirewrapped to these pins.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Counter/Timer CLK2 source is OPT0, SBX A	5-6
Counter/Timer CLK2 source is OPT0, SBX B	3-4
Counter/Timer CLK2 is 1.2288 MHz	1-2**

**As shipped

Figure 2-18. Counter/Timer Chan. 2 Clock Source Select, Jumper W6

Section 3
OPERATION AND PROGRAMMING

INTRODUCTION

This section includes a general discussion of multimaster STD BUS system operation, the operation of the 7864 Multimaster CPU/SBX card, and the programming required to initialize and use the 7864 onboard functions. These functions include the reset circuit, interrupts, memory and I/O addressing, the 8259A Interrupt Controller, and the 8253-5 Counter/Timer.

SINGLE-CPU SYSTEMS

The 7864 can be used as the sole CPU card in a system in the same way that STD BUS systems have always been implemented in the past — with only one CPU card in the card rack. Certain jumpers on the card should be configured for single-CPU system operation as described in Section 2 under Multimaster Configuration Jumpers. Operation and programming are the same as described in the following except that bus arbitration is obviously not required; the 7864 always controls the STD BUS (unless DMA operations are used) and wait states for bus arbitration are never needed for STD BUS memory or I/O access.

MULTIMASTER STD BUS SYSTEMS

The 7864 has the required onboard bus arbiter that allows its use in multimaster STD BUS systems. Up to sixteen 7864 or other multimaster CPU cards can be installed in the same card rack, each executing its own program independently while sharing common bus resources. These common or "global" resources include any memory or I/O not located on a multimaster card.

Bus arbitration is done entirely in hardware and is essentially transparent to the program being executed by each of the multimasters. An understanding of the arbitration process can be helpful to the user in setting up an efficient bus protocol for the multimaster system. This protocol is defined by user-provided software and allows the multimaster cards to communicate and to coordinate tasks.

Bus Arbitration

When a multimaster card is executing programs from or otherwise accessing its own onboard memory, or using onboard I/O, it does not need control of the STD BUS. Control of the STD BUS is only required to access global memory or I/O and only one multimaster can have control of the STD BUS at any one time to access these global resources. Multimaster cards usually have significant amounts of onboard memory and I/O (the 7864 can have up to 128K of memory, an Interrupt Controller, a Counter/Timer, two user-supplied SBX I/O modules, and the optional 8087 Math Coprocessor onboard) so that each can perform complex system functions without the need to continually access global memory.

When a multimaster executes a memory or I/O cycle that requires access to off-card (global) memory or I/O and does not at that time have control of the STD BUS, its bus arbiter holds the CPU in a wait state until it can gain access to the bus. The length of time that the wait state is held, i.e., until any given multimaster can gain access to the STD BUS and continue program execution, depends on several factors.

If the multimaster requesting bus access was the last multimaster to have control of the bus (no other multimaster has needed to access global memory or I/O since its last global access), it still has control of the bus and no wait states are required. If another multimaster is currently using the bus, that multimaster relinquishes the bus at the end of its current machine cycle and, after one bus arbitration cycle (three CNTRL* clock cycles), the requesting multimaster has control of the STD BUS, the wait state is released, and program execution continues with the global memory or I/O operation that started the bus arbitration process.

Simultaneous bus access requirements from more than one multimaster are prioritized by the bus arbiters themselves, using the STD BUS priority chain. Each multimaster (starting with highest priority or rightmost) has control of the bus for one memory or I/O cycle and then relinquishes the bus to the next lower priority multimaster. If (n) multimasters request access simultaneously, the longest that the lowest priority multimaster will be held in a wait state before being released to execute one bus memory or I/O cycle is (n-1) 8088 machine cycles plus (n) bus arbitration cycles (plus the time it takes for the multimaster originally controlling the bus to complete its cycle in progress). Any other multimaster attempting to gain access to the bus will be held in a wait state until all the multimasters which simultaneously requested bus access have had access to the bus for one cycle.

With this bus arbitration scheme, it is likely that any time a multimaster tries to access global memory or I/O it will first be held in a wait state for some period of time. If fast program execution is necessary, the number of bus accesses should be minimized. Generally, programs being executed by a multimaster should reside in onboard memory (either RAM or ROM), since execution of programs from global memory would require a bus access to read each instruction. If more than one multimaster were executing programs from global memory, speed of program execution would be greatly reduced since each would have to alternate fetching instructions with the other multimasters with the added delay of a bus arbitration cycle each time control of the bus changed hands.

Bus Lock

Multimasters have the capability of "locking" the bus, i.e., retaining control of the bus instead of relinquishing it at the end of any machine cycle during which another multimaster requires bus access. A multimaster can lock the bus either with software (by inserting a lock prefix to an instruction in the program) or with hardware (by setting an output port bit). The bus will be locked when the multimaster implementing a lock mode gains control of the bus through the normal bus arbitration process.

Any multimaster attempting a bus access while the bus is locked by another multimaster will be held in a wait state until the lock is removed. If the bus has been locked with the software lock mode, it remains locked until the multimaster which locked it has completed execution of the instruction with the lock prefix. If the bus has been locked with hardware, it remains locked until the multimaster that locked the bus clears its lock output port bit.

Any multimaster can implement Software Lock or Hardware Lock modes as required. The highest priority multimaster (the rightmost in the card rack) can also use a slightly different type of hardware lock called DMA Lock. This mode is the same as Hardware Lock except that while DMA Lock mode is active, the STD BUS signals BUSRQ* and BUSAK* can be used in the usual way by DMA controllers on non-multimaster STD cards. Traditional STD BUS DMA operations are possible only when DMA Lock mode is active since multimaster bus arbiters use BUSRQ*/ BUSAK* in a different way from normal DMA controllers (BUSAK* active indicates that the bus is being used by a multimaster instead of indicating that the bus is available for use by the device that supplied BUSRQ*). This restriction on the use of DMA controllers is not usually a significant limitation in a multimaster STD BUS system since each multimaster always has direct access to all global system memory and I/O. One multimaster can, in effect, handle DMA tasks for another.

As noted above, any multimaster attempting a bus access while a lock mode is active is held in a wait state until the lock mode has been cleared by the multimaster currently using the bus. The use of lock modes should be carefully considered by the program designer who must ensure that no time-critical function is affected by a bus lock. It may be desirable to limit the duration of a Hardware or DMA lock, either in software or with timer-generated interrupts, so that other multimasters are not denied access to the bus (and held in a wait state) for too long. The 7864 onboard counter/timer can be used for this purpose.

Multimaster System Configurations

The interface between multimasters is well defined from a hardware standpoint by the bus arbitration scheme, yet flexible enough to support a variety of different system configurations. The way multimasters operate together in the system is mainly dependent upon software written by the user.

A multimaster system can be set up in a conventional master-slave configuration in which one multimaster is designated (in software) as the master and all others as slaves. The master off-loads specific tasks to specific slaves: one slave may be used exclusively for communications, another for arithmetic computation, another for data acquisition, and so on. Writing the software for such a system might be simpler than for an equivalent single-CPU system (since each multimaster has only a portion of the overall system task to perform) and throughput could be greatly increased since all lower-level tasks would be executed in parallel by the slave multimasters.

In another possible system configuration, two or more multimasters might run entirely unrelated programs and treat other cards on the STD BUS as shared resources. These might include other multimasters as well as memory and/or I/O cards. In such a system, several "resource" multimasters might be used for exactly the same function: they could perform computations for each of the "masters" in the system as needed since each can have its own onboard 8087 math coprocessor.

BUS PROTOCOL (Communication Between Multimasters)

The hardware interface is very flexible and places few restrictions on system configuration. Therefore, the bus protocol that defines the way in which multimasters communicate on the bus can be designed by the user and implemented in software.

Shared Memory (Mailboxes)

Communication between multimasters in an STD BUS system is usually through global memory (memory not located on a multimaster but on a separate memory card). Most of this global memory is directly addressable by all multimasters (see the subsection on memory and I/O addressing following). Certain areas in global read/write (RAM) memory can be designated by the program designer as "mailboxes" where commands, status information, and data can be written by one multimaster and read by another.

The 8088 XCHG (exchange) instruction can be used to pass commands and/or status information between two multimasters. This instruction switches the contents of source and destination operands. When this instruction is used for multimaster communication, one operand is a register in the multimaster's CPU and the other operand is a global read/write memory mailbox location. The XCHG instruction can be used with the LOCK prefix to implement the Software Lock mode described above. This ensures that no other multimaster can access (change) the memory location operand while the exchange is actually taking place.

Figures 3-1 through 3-3 show some examples of how the XCHG instruction with LOCK prefix can be used in multimaster communications. In Figure 3-1, a byte labeled "CNTRL1" has previously been defined in global RAM memory and serves as an access control flag for some global bus resource (an I/O device, a block of memory, etc.). If CNTRL1=0, the resource is available for use; if CNTRL1=1, another multimaster is using the resource. The program shown in Figure 3-1 would be executed by any multimaster requiring use of the resource. The multimaster would wait in the loop at the beginning of the code until CNTRL1=0. The use of the LOCK prefix to the XCHG instruction prevents more than one multimaster from changing the access control flag from 0 to 1 (i.e., getting control of the resource) at one time.

```
;This is a location in global RAM:

CNTRL1      DB      0           ;Access control flag for global resource

;Any multimaster requiring use of the resource executes this program:

CHECK:      MOV     AL,1        ;Set AL to 1
     LOCK   XCHG    CNTRL1,AL   ;Exchange contents of AL and CNTRL1
            TEST    AL,AL       ;Set Z flag if CNTRL1 was 0
            JNZ     CHECK       ;Retry if CNTRL1 was not 0
             -                  ;CNTRL1 was 0 and is now 1
             -                  ;      This multimaster now has control
             -                  ;      of resource, and can continue
             -                  ;      operation
            MOV     CNTRL1,0    ;Operation completed - clear CNTRL1 so
                                ;      other multimasters can use resource
```

Figure 3-1. Use of XCHG Instruction with Lock Prefix

Figure 3-2 shows how two access control flags can be used to control a swing buffer for one-way communication of blocks of data between two multimasters. The buffer is split into two halves, each having a separate access control flag. If an access control flag equals 0, the associated half of the buffer has been emptied by the receiving multimaster and the transmitting multimaster can move more data into it. If the flag equals 1, the associated half-buffer has been filled by the transmitting multimaster (using the LOCK XCHG instruction) after it has moved a block of data into an empty half-buffer. The flag is cleared by the receiving multimaster (with LOCK XCHG) after it has read the data in from a full half-buffer. The advantage of using a swing buffer is that both multimasters can be moving data simultaneously into and out of the buffer without having to wait for the other to finish its operation.

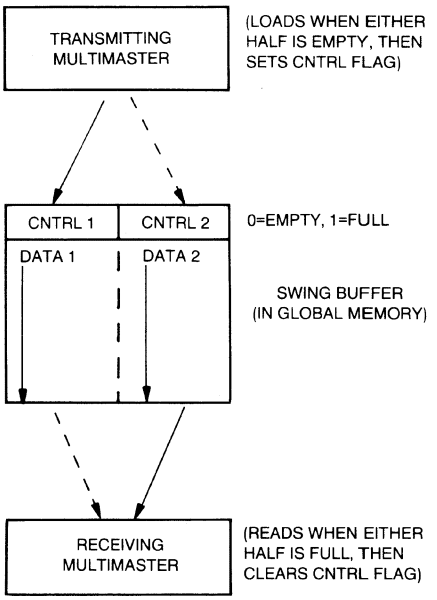


Figure 3-2. Multimaster Swing Buffer

Software Interrupts

Figure 3-3 shows how the XCHG instruction could be used in conjunction with the software interrupt instruction (INT n, where n = interrupt type number) to pass commands between multimasters. Figure 3-3a shows programs executed by one multimaster and Figure 3-3b shows programs executed by any other multimaster that needs to communicate with the first.

```
;All multimasters can access this block of global RAM:

CNTRL2          DB      Ø               ;This is the flag for access control
CMD_1           PROC FAR                ;Subroutine executed by 1st multimaster
                DB      ØFØH            ;Code for a LOCK prefix instruction
INSTR           DW      ØBB87H          ;Code for a two byte NOP instruction
                                          (i.e. XCHG  BX,BX)
                RET                     ;Return from subroutine
CMD_1           ENDP                    ;

;1st multimaster periodically executes this instruction:

                CALL    CMD_1           ;Execute subroutine in global RAM

;After another multimaster has moved "INT n" code to INSTR, the next CALL
;     CMD_1 will cause an INT n
;The 4-byte interrupt vector table entry at Address ØØØØ:(n*4) is the
;     offset and segment of this interrupt service routine:

INTn_SVC        PROC FAR                ;Interrupt Service Routine
                 -                      ;(Instructions are inserted here which
                 -                      ;     perform the actual interrupt
                 -                      ;     service operations)
                MOV     INSTR,ØBB87H    ;Replace INT n code with a two byte NOP instruction
                                          (XCHG  BX,BX)
                MOV     CNTRL2,Ø        ;Clear access control flag
                IRET                    ;Return from interrupt n service
INTn_SVC        ENDP                    ;
```

A) FIRST MULTIMASTER'S PROGRAM

```
;All multimasters can access this block of global RAM:

CNTRL2          DB      Ø               ;This is the flag for access control
CMD_1           PROC FAR                ;Subroutine executed by 1st multimaster
                DB      ØFØH            ;Code for a LOCK prefix instruction
INSTR           DW      ØBB87H          ;Code for a two byte NOP instruction (XCHG  BX,BX)
                RET                     ;Return from subroutine
CMD_1           ENDP                    ;

;To cause 1st multimaster to execute an INT n (n = type number, 32 to 255),
;     another multimaster executes this program:

WAIT:           MOV     AL,1            ;Try to set access control flag
     LOCK       XCHG    CNTRL2,AL       ;
                TEST    AL,AL           ;Wait until CNTRL2 equaled Ø during XCHG
                JNZ     WAIT            ;
                 -                      ;(Insert additional instructions here-
                 -                      ;     set up data to be passed, etc.)
     LOCK       MOV     INSTR,nCDH      ;Move code for INT n to RAM
```

B) ANY OTHER MULTIMASTER'S
WITH SOFTWARE INTERRUPTS

Figure 3-3. Multimaster Communication with Software Interrupts

The programs for both multimasters define a five-byte area in global RAM. The first byte is an access control flag similar to that previously described, while the following four bytes are a subroutine (CMD1, Figure 8) that will be periodically executed by the first multimaster. Three bytes must be initialized so that if the subroutine is called by the first multimaster it will execute a locked two-byte no-operation instruction (XCHG BX,BX) and an inter-segment return (RET) while waiting for another multimaster to communicate.

When another multimaster needs to communicate with the first, it replaces the no-operation instruction (XCHG BX,BX) with an INT n instruction. The first multimaster's program executes the INT n instruction the next time the subroutine CMD__1 is called. The INT n service routine takes whatever action is predefined and then replaces the INT n with a two-byte no-operation instruction and clears the access control flag, allowing another multimaster to repeat the communication procedure as needed. Using the LOCK prefix ensures that only one multimaster at a time can use this procedure.

The use of software interrupts is an efficient method of multimaster communication. Since n (the interrupt type number) can be any value between 32 and 255, many commands can be implemented by writing an appropriate interrupt service routine for each without the need for polling.

An access control flag (CNTRL2) can also be used to control access to a block of global memory which serves as the mailbox for passing data or parameters required by the specific command.

Periodic STD BUS Access

Each multimaster periodically reads or executes code from global read/write memory to see if new commands, status information, or data are being sent to it from another multimaster. The frequency of bus access for this purpose depends upon the system configuration and the particular application. In a master/slave/smart I/O system, each slave might not access its global memory mailboxes until it had completed an assigned task. At that time, it would move the results (if any) and "task-completed" status into the appropriate mailboxes and then continually monitor its command mailbox, waiting for a new task to be assigned. The "master" multimaster in the same system would scan the slaves' status mailboxes, utilize the results from slave operations when available, and assign new tasks to the slaves as tasks were completed.

Interrupts

Onboard periodic interrupts on each multimaster could determine the frequency of bus access for reading command or status mailboxes. Multimasters with an onboard timer function (7864) that can generate an interrupt, could check the appropriate mailboxes, or execute a program in global memory when interrupted. The 7864 counter/ timer can be used for this purpose. This timed approach would be useful in a true multimaster system where each multimaster might periodically check to see what bus resources were available for use.

Figure 3-4 shows how periodic interrupts could be used with the software interrupts described above. The code is similar to that in Figure 3-3, except that the subroutine in global RAM executed by the first multimaster is now the interrupt service routine for the periodic hardware interrupt INT x. Another multimaster needing to communicate with the first executes the program shown in Figure 3-3b, causing the first multimaster to execute a software INT n at the time of the next periodic hardware interrupt.

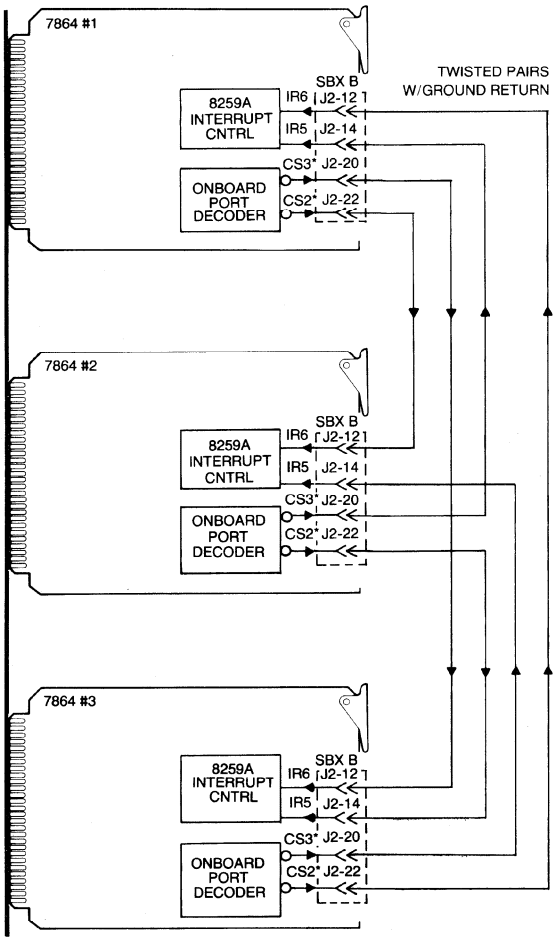
```
;All multimasters can access this block of global RAM:

CNTRL2      DB      Ø           ;This is the flag for access control
INTx_SVC    PROC                ;Interrupt service routine for 1st multimaster
            DB      ØFØH        ;Code for A LOCK prefix instruction
INSTR       DW      ØBB87H      ;Code for a two byte NOP instruction (XCHG  BX,BX)
            IRET                ;Return from interrupt
INTx_SVC    ENDP                ;

;1st multimaster periodically gets an interrupt from hardware which
;     supplies the vector x, causing an INT x
;The 4-byte interrupt vector table entry at Address ØØØØ:(x*4) is the
;     offset and segment of INTx_SVC, the interrupt service routine

;After another multimaster has moved "INT n" code to INSTR, the next
;     hardware INT x interrupt service will cause a software INT n
;The 4-byte interrupt vector table entry at Address ØØØØ:(n*4) is the
;     offset and segment of this interrupt service routine:

INTn_SVC:   -                   ;(Instructions are inserted here which
            -                   ;     perform the actual interrupt
            -                   ;     service operations)
            MOV     INSTR,ØBB87H;Replace INT n code with a two byte NOP
                                  instruction (XCHG  BX,BX)
            MOV     CNTRL2,Ø    ;Clear access control flag
            IRET                ;Return from interrupt n service
```

Figure 3-4. Communications with Periodic Interrupts

An I/O card that can generate periodic bus interrupts (INTRQ* on the STD BUS) such as Pro-Log's 7308 Counter/Timer card could perform the same function. The 7308 does not provide an 8088 interrupt vector, so each multimaster must provide its own vector on-card when responding to an STD BUS INTRQ*. Each multimaster would respond to the bus interrupt by accessing its mailboxes to see if updated commands, status, or data were available to it. If faster response to some command were required, a multimaster could use the 7308 to generate an almost immediate bus interrupt by programming another counter/timer channel to down-count from a count of one and enabling the interrupt from that channel.

Direct Interrupts Between Multimasters

If direct hardware interrupts between multimasters are required for the fastest possible multimaster communication response, the SBX connectors can be used. Each connector has two interrupt input lines to the onboard 8259A Interrupt Controller. These lines could be driven by another multimaster, either with I/O lines or (if the interrupting multimaster is another 7864) with the SBX chip select signals. These interrupt line connections would have to be made across the front of the card rack. Figure 3-5 shows a multimaster system with three 7864 cards. Using J2, SBX Connector B on each card, each processor can interrupt either of the other two by doing a dummy read or write to I/O ports mapped onto its SBX connector. Any such I/O operation strobes the SBX chip select outputs, which are directly connected to the rising-edge-sensitive interrupt input lines on the other cards.



NOTE:

CS2* ACTIVE DURING I/O READ OR WRITE TO PORTS FFD0-FFD7

CS3* ACTIVE DURING I/O READ OR WRITE TO PORTS FFD8-FFDF

Figure 3-5. Hardware Interrupts between Multimasters

Output port lines (or 7864 SBX Chip Select signals) could also be connected to the interrupt inputs of Pro-Log's 7320 Priority Interrupt Controller Card that can generate an STD BUS INTRQ*. One multimaster in the system could get its interrupt vector directly from the 7320 by executing an STD BUS interrupt acknowledge cycle. (The 7320 would be configured so the interrupt request is cleared by software instead of by INTAK* from the processor.) Any other multimaster responding to STD BUS INTRQ* would have to provide its own onboard interrupt vector.

OPERATION AND PROGRAMMING

Reset

The 7864 resets the 8088 CPU, the 8087 Math Coprocessor, and certain onboard logic (including the bus arbiter) upon entering a reset state. The STD BUS signal SYSRESET* is also driven active (low) during this time. The source of the reset can be either the onboard power-on/DC power-fail circuitry or pushbutton or system reset from the STD BUS.

Power-on/DC Power-Fail Reset

The 7864 uses a precision voltage reference and comparator to monitor the level of Vcc on-card. During power-on, the reset state is held for 60 milliseconds after Vcc has reached 4.75V minimum. This ensures that all components on the card are operating within specification (Vcc = 5V ± 5%) when reset is released. Reset is also asserted when Vcc on-card falls below a specified level. Refer to Section 1, Electrical Specifications, for exact voltage levels and tolerances. Under certain conditions, adjustment of the power supply or a jumper change in the reset circuit may be required before reset will be released and the 7864 begins operation. See the jumper reset options in Section 2, Installation.

Pushbutton Reset

The 7864 can be forced into a reset state with an active (low) level on the STD BUS pushbutton reset (PBRESET*) signal. PBRESET* can be either controlled by a switch or driven with an open collector device. The signal is debounced on-card and must remain low for a minimum of 5 milliseconds to guarantee a reset.

System Reset

An active (low) level on the STD BUS system reset signal (SYSRESET*) will also cause a 7864 reset. (The 7864 will not drive SYSRESET* in response to this reset.) This signal is not debounced and should be driven only by circuitry specifically designed for this purpose (such as an AC power-fail detect card or the reset circuitry on other multimasters).

In a multimaster system, SYSRESET* is not released until the power-on circuits on all multimasters have sensed the correct Vcc level and completed their time delays, thus assuring that all multimasters start program execution simultaneously. Similarly, if any multimaster detects a DC power-fail condition, all multimasters are reset by SYSRESET*. Refer to Section 1, Electrical Specifications, and Section 2, Reset Jumper W5, for voltage levels and other reset considerations.

When reset is released, program execution begins at physical address FFFF0 hex (code segment = FFFF hex, instruction pointer = 0000 hex).

Interrupts

Every 8088 interrupt has a type number that identifies it to the CPU. The type number is used in the 8088 vectored interrupt scheme. It is a single-byte value that the CPU internally multiplies by four to form a pointer. The pointer points to an interrupt table in segment 0000 hex containing the address of the interrupt service routine. The multiplication of the type number (vector) by four allows the complete physical address (Code Segment and Instruction Pointer, two 16-bit numbers) of the interrupt service routine to be stored in the interrupt table as four consectuive bytes.

The 7864 8088 CPU can respond to both internal and external (to the CPU) interrupts. Sources for external interrupts on the 7864 can include the STD BUS signals NMIRQ* (nonmaskable interrupt request) and the INTRQ* (interrupt request) and the onboard 8259A Interrupt Controller.

Nonmaskable interrupt requests on the STD BUS NMIRQ* signal are predefined by the 8088 as Type 2 interrupts and no other vector is needed. Figure 3-6 shows how the CPU processes an NMIRQ*. A Type 2 interrupt has a higher priority than any other external interrupt and since it is nonmaskable (the CPU always responds to a Type 2 interrupt at the end of its current instruction cycle), NMIRQ* is generally used to signal the CPU of a "catastrophic" event such as the imminent loss of power or a parity error.

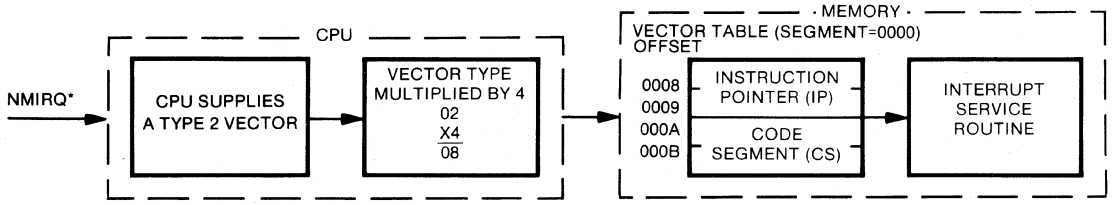


Figure 3-6. NMIRQ* Processing

Interrupt requests on the STD BUS INTRQ* signal and from the onboard Interrupt Controller are not assigned a type number by the CPU. The interrupting device must provide the type number (or vector) on the CPU's data bus during the interrupt acknowledge cycle. Figure 3-7 shows how the 8088 processes these interrupts. The 7864 differentiates between STD BUS INTRQ* and interrupt requests from the onboard Interrupt Controller; INTRQ* has a higher priority than onboard interrupts. When the 7864 responds to an onboard interrupt request, it is assumed that the vector will be generated on-card (by the Interrupt Controller) and an STD BUS access is not attempted during the interrupt acknowledge cycle.

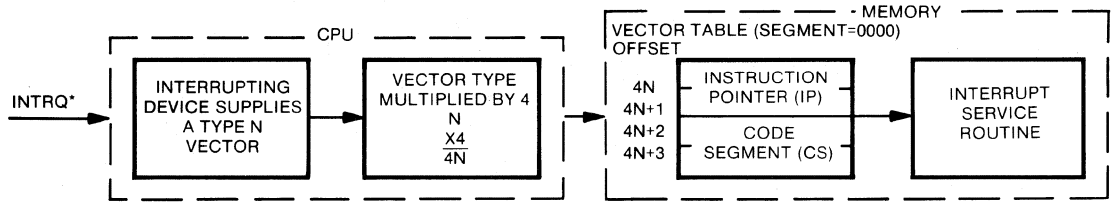


Figure 3-7. INTRQ* Processing

In multimaster systems, only one CPU card can normally respond to an STD BUS INTRQ* by gaining bus access, executing an interrupt acknowledge cycle, and reading the type number (vector) supplied by the interrupting device from the STD BUS data bus. (If more than one multimaster executed an interrupt acknowledge cycle on the STD BUS, only the highest priority would get a vector since most peripheral devices only put out a vector once when the interrupt is first acknowledged.)

If other multimasters are to respond to an STD BUS INTRQ*, they must each generate a vector onboard. This capability is provided on the 7864 since INTRQ* is connected (through a buffer) to one input of the Interrupt Controller. The controller can generate an interrupt when INTRQ* is active and provides the required on-card vector when the interrupt is acknowledged. This onboard vector capability allows the use of cards that can generate INTRQ* but not an 8088 vector in a 7864 system. All 7864 cards would respond to INTRQ* in this way. The shorting connector should be removed from Jumper W9 if this onboard INTRQ* response is to be used, so that the 7864 does not respond to an STD BUS INTRQ* with a bus interrupt acknowledge cycle.

If the shorting connector is removed from Jumper W3 on the 7864, the card will not respond to STD BUS INTRQ* at all. Refer to Interrupt Options in Section 2 for more information on maskable interrupt response.

The 8087 Math Coprocessor can generate interrupts when certain internal conditions or "exceptions" (such as stack overflow or underflow or indeterminate operations such as divide by zero) are detected. The 8087 interrupt output drives one input of the Interrupt Controller, which provides an on-card interrupt and vector for 8087 interrupts. Other onboard interrupts can be generated through the Interrupt Controller by the counter/timer and by the user-supplied SBX I/O modules. See the section following on Interrupt Controller operation and programming.

Memory Addressing

The 7864 8088 CPU provides a 20-bit memory address during each memory operation so the 7864 can direct address 2^{20} (1,048,576 or 1M) bytes of memory. The two onboard memory sockets can be configured to support various sizes of memory devices and can be mapped at different locations within the one megabyte memory map. See Figure 2-13 for onboard memory mapping options. Generally, one memory socket is mapped at the high end of memory to support the 8088 power-on restart address (FFFF0 hex) while the other is mapped at the low end to include the 8088 interrupt vector table (00000 to 007FF hex).

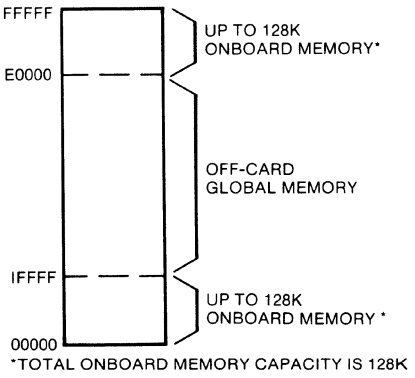
In a multimaster system, the 7864 can address its onboard memory and continue program execution while the STD BUS is being used by another multimaster; it does not need control of the bus. The 7864 needs access to (and may have to arbitrate for) the STD BUS only when addressing memory that is not mapped into its onboard sockets. In addition, no other multimaster can ever access the 7864 onboard memory.

A block of global memory may be mapped at the same address as any multimaster's onboard memory, but it cannot be used by any multimaster. (This situation is unavoidable when using high-capacity dynamic RAM cards such as the 7712 in Figure 3-8c). When a 7864 currently controlling the STD BUS accesses its onboard memory, it puts out the address and control signals onto the STD BUS. The data bus buffer is not enabled and there is no bus contention, but the contents of global RAM memory at that address will be altered by write operations.

When the 7864 is addressing off-card or global memory (in a multimaster system when it has control of the STD BUS), the lower 16 address bits are output on address lines A0-A15 on the STD BUS. The upper four bits (A16-A19) are time multiplexed onto the STD data bus (bits D0-D3) at the beginning of each machine cycle. Memory cards used in 8088 STD systems latch these upper address lines on the rising edge of STD BUS control signal MCSYNC*.

MEMEX is defined in the 8088 STD BUS specification as an enable for memory cards that only decode a 16-bit memory address. No provision is made for driving MEMEX on the 7864 and only memory cards with the onboard latch required to decode the full 20-bit 8088 address should be used with the 7864 to avoid redundant addressing of memory.

Several examples of memory mapping in 7864 STD systems, both single-CPU and multimaster, are shown in Figure 3-8. Note that in multimaster systems the high and low ends of the memory map are usually the onboard memory exclusively available to each multimaster and most of the memory map (always at least 792K bytes when using 7864s as multimasters) is available as common or global memory.



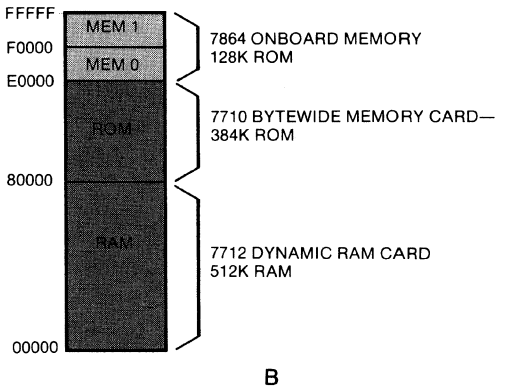
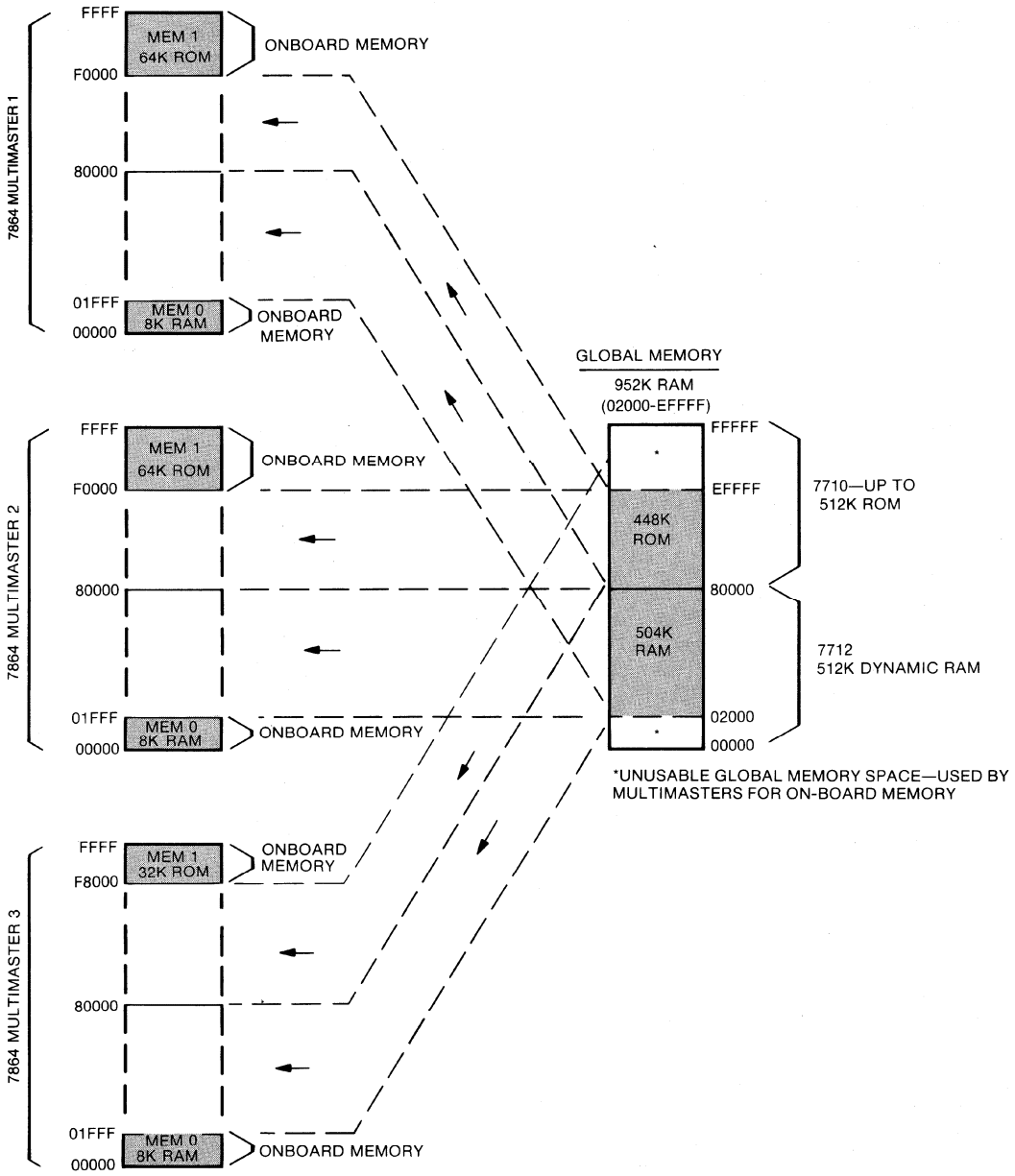


Figure 3-8. Memory Mapping Examples
(Continued on Next Page)



C

Figure 3-8 (Continued)

I/O Addressing

The 7864 8088 CPU provides a 16-bit I/O port address during each I/O operation and can directly address 2^{16} (65,536 or 64K) I/O port locations. As with memory, onboard I/O (the Interrupt Controller, Counter/Timer, SBX modules, and bus lock port) can be read from or written to without having access to the STD BUS. Also like onboard memory, these onboard ports are not accessible to any other multimaster in the system. The 7864 onboard bus lock port is mapped at Port FFFF hex. When bit D0 is set, the lock mode selected (either Hardware or DMA Lock) is active and when bit D0 is cleared, the bus lock is released. Bits D1-D7 are not used.

Due to onboard decoding limitations, the upper 8K of the 64K I/O address field is reserved for onboard I/O even though only 38 port addresses are actually used. The lower 56K (Ports 0000-DFFF hex) is available for common or global I/O that can be addressed by all multimasters in the system. See Figure 1-5 for 7864 I/O mapping. Figure 3-9 shows the mapping of user-supplied SBX modules when installed in SBX connectors A and B. Note that Ports E000-FFBF, FFE0-FFE7, FFEC-FFEF, and FFF2-FFFE hex should never be accessed since the onboard I/O devices will be redundantly addressed in these address ranges.

Most existing STD BUS I/O cards decode only an 8- or 10-bit I/O address since few systems need more than 256 or 1024 ports. The full port address range of these cards (00-FF for 8-bit or 000-3FF for 10-bit) is available for global I/O in a 7864 system. Indirect (16-bit) addressing should be used when addressing 10-bit I/O cards to allow the card to distinguish between onboard and off-card ports; 8-bit I/O cards can be directly addressed in Page 0 of the I/O address space. Eight- and ten-bit I/O cards are not usually used together in the same system since port addresses would have to be selected with great care to avoid redundant addressing ("shadow" ports). Provision is made for grounding the STD BUS IOEXP signal onboard the 7864 since many 8-bit address I/O cards use this signal as an enable input. Several examples of I/O port configurations in 7864 systems are shown in Figure 3-10.

SBX MODULE	SBX CHIP SELECT	I/O ADDRESS RANGE
A	MCS0*	FFC0-FFC7
	MCS1*	FFC8-FFCF
B	MCS0*	FFD0-FFD7
	MCS1*	FFD8-FFDF

Figure 3-9. SBX Module Mapping

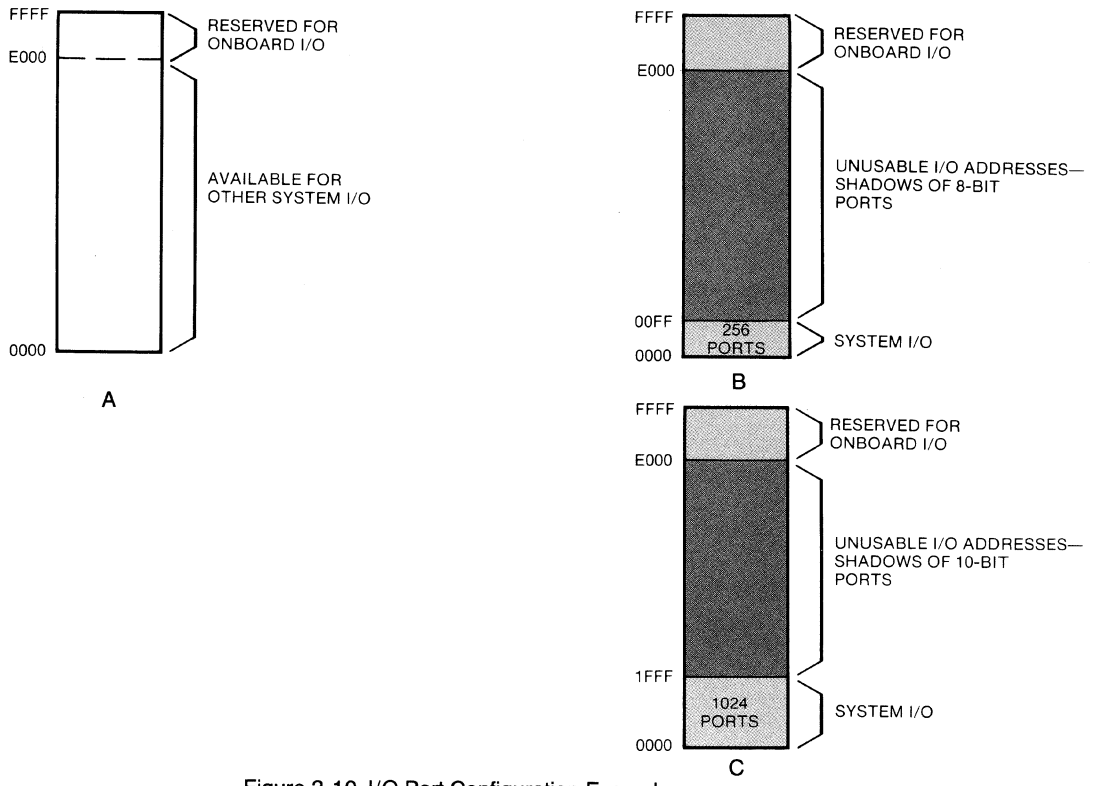
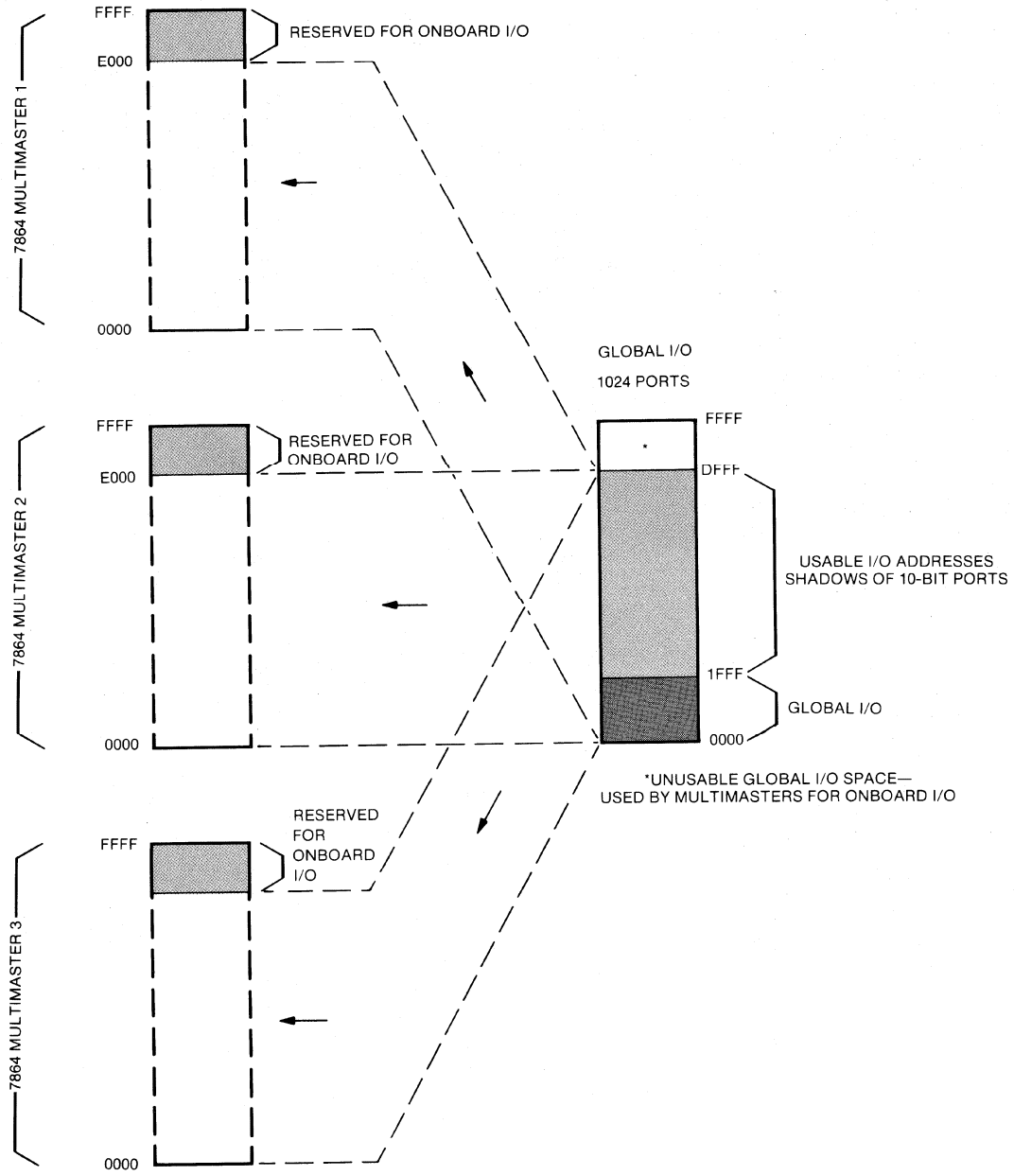


Figure 3-10. I/O Port Configuration Examples



D

Figure 3-10. (Continued)

8253-5 COUNTER/TIMER

The onboard Counter/Timer has three independent 16-bit counter/timer channels. Each is dedicated to a specific function on the 7864; therefore, only the valid operating modes for each channel are described in the following paragraphs. For further information, refer to Intel's Microsystem Components Handbook, Volume II.

Channel 0: Interrupt Timer

This channel is used in conjunction with the Interrupt Controller to generate periodic or delayed interrupts. In a multimaster system, these timed interrupts can be useful in establishing a bus protocol: the interrupt can be used to determine the frequency of bus access or to limit the duration of a hardware bus lock.

The output from channel 0 is connected to interrupt input IR1 on the Interrupt Controller, which must be initialized and programmed to generate the actual interrupt to the 8088 and to provide the required type number or vector during the interrupt acknowledge cycle. (See the subheading 8259A Interrupt Controller following this subsection.)

To generate a single delayed interrupt, channel 0 must be initialized by writing the following bytes to the ports indicated:

PORT	BYTE	DESCRIPTION
FFEB	30H	Mode 0 for channel 0
FFE8	XXH	LSB Least Significant Byte of count
FFE8	XXH	MSB Most Significant Byte of count

The count is a number between 0000 and FFFF hex. The delay starts as soon as the MSB is written to Port FFE8; the timer counts down and generates an interrupt when the count goes to zero. To determine the count, divide the delay required by 813.8 nanoseconds and convert the result to hexadecimal. The maximum delay possible is 65536 times 813.8 nanoseconds, or 53.33 milliseconds. (This longest delay results from loading a count of hex 0000, which appears as a count of 10000 to the device.) To generate another interrupt, the two-byte count (or a different count for a different delay) must be reloaded.

A periodic interrupt can be generated by initializing channel 0 with the following bytes:

PORT	BYTE	DESCRIPTION
FFEB	34H	Mode 2 for channel 0
FFE8	XXH	LSB of count
FFE8	XXH	MSB of count

Operation is the same as described above, except that the count is reloaded after zero count is reached and the entire process is repeated automatically.

Channel 1: Programmable SBX Clock

The output of Counter/Timer channel 1 can be connected (through a jumper) to Option Line OPT1 on one or both SBX connectors and can provide a programmable clock for SBX modules.

To start the clock, channel 1 must be initialized by writing the following bytes to the ports indicated:

PORT	BYTE	DESCRIPTION
FFEB	76H	Mode 3 for channel 1
FFE9	XXH	LSB of divisor
FFE9	XXH	MSB of divisor

The output of channel 1 will be a square wave, the frequency being dependent upon the two divisor bytes. To determine these bytes, divide the desired clock period by 813.8 nanoseconds and convert the result to hexadecimal. Divisors of hex 0001 and 0003 cannot be used; a divisor of 0000 hex appears to the device as 10000 and results in the slowest possible clock.

This programmed clock has a frequency range of 18.75 to 614400 Hertz, although since only integers can be loaded as the divisor the actual number of frequencies available toward the high end of this range is limited.

Channel 2: SBX Counter

The clock input to channel 2 of the Counter/Timer can be connected through a jumper to Option Line OPT0 of either SBX connector A or B providing an event counter function for either SBX module. The output from channel 2 is connected to one of the interrupt inputs of the Interrupt Controller, which can be programmed to provide an 8088 interrupt after the programmed number of events have been counted. See the following section for Interrupt Controller initialization and programming.

To start the counter function, the following bytes must be written to the ports indicated:

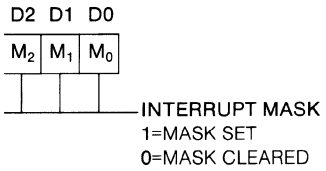
PORT	BYTE	DESCRIPTION
FFEB	B0H	Mode 0 for channel 2
FFEA	XXH	LSB of count
FFEA	XXH	MSB of count

; to STD BUS interrupt requests
:ecuting an interrupt acknowledge
nd reading a vector from the STD
: Interrupt Controller generate the
ıe vector on-card, since INTRQ* is
terrupt Controller. (See Section 2,
TD BUS interrupt acknowledge is
NTRQ* has a higher priority than
errupt Controller. Priority of STD
upt Controller interrupts is estab-
terrupt control PAL. The lower-
st from the Interrupt Controller is
ıigher-priority INTRQ* is acknowl-
d be masked if STD BUS INTRQ*
:e OCW1 following).

Words

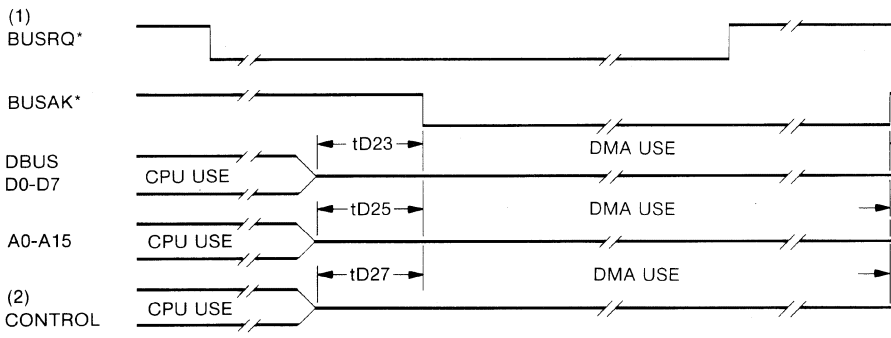
vritten to the Interrupt Controller,
:cept interrupt requests at its input
scribed above. However, during
modes can be selected by writing
ds (OCWs). Each of the tree OCWs
rupt Controller operation is dis-
following paragraphs.

ars the mask bits in the Interrupt
7-M0 represent the eight mask bits.
rrupts from the corresponding IR
indicates that the corresponding IR
'1 is issued to the Interrupt Con-
to Port FFF1 hex.



CW1 (Output Port FFF1 Hex)

Rotate and End of Interrupt modes
the two. OCW2 commands are
Controller by writing a byte having
FF0 hex.



SYMBOL	PARAMETER
tD23	Delay from Data Bus 3-state to BUSAK*
tD24	Delay from BUSAK* to Data Bus driven
tD25	Delay from Address Bus 3-state to BUSAK*
tD26	Delay from BUSAK* to Address Bus driven
tD27	Delay from Control Bus 3-state to BUSAK*
tD28	Delay from BUSAK* to Control Bus driven

All times given in nanoseconds.

Figure 1-13. Bus Exchange Timing

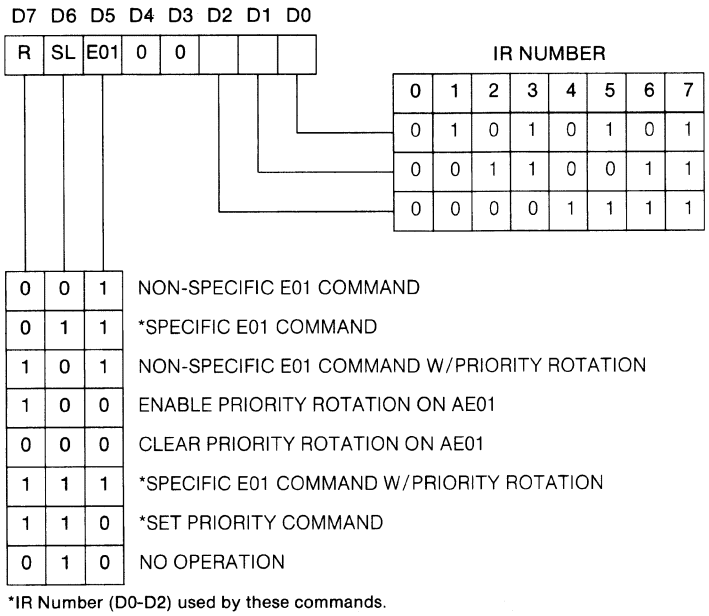

D7 D6 D5 D4 D3 D2 D1 D0
R SL E01 0 0
IR NUMBER
0 1 2 3 4 5 6 7
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1
0 0 1 NON-SPECIFIC E01 COMMAND
0 1 1 *SPECIFIC E01 COMMAND
1 0 1 NON-SPECIFIC E01 COMMAND W/PRIORITY ROTATION
1 0 0 ENABLE PRIORITY ROTATION ON AE01
0 0 0 CLEAR PRIORITY ROTATION ON AE01
1 1 1 *SPECIFIC E01 COMMAND W/PRIORITY ROTATION
1 1 0 *SET PRIORITY COMMAND
0 1 0 NO OPERATION
*IR Number (D0-D2) used by these commands.

Figure 3-14. OCW2 (Output Port FFF0 Hex)

End of Interrupt (EOI)

The In Service (IS) bit can be reset by a command word that is written to OCW2 before returning from an interrupt service routine (an EOI command) or the IS bit can be reset automatically at the end of the interrupt acknowledge cycle (see Automatic End of Interrupt following). There are two forms of EOI commands: Specific and Nonspecific. When the Interrupt Controller is operating in the Fully Nested mode, it can determine which IS bit to reset upon receiving an EOI. When a Nonspecific EOI command is written to OCW2, the Interrupt Controller automatically resets the highest IS bit of those that are set since, in the Fully Nested mode, the highest IS bit was necessarily the last interrupt acknowledged and serviced. A Nonspecific EOI command can be issued by writing a 20 hex to Port FFF0.

When a mode other than the Fully Nested mode is used (Special Mask mode, Rotating Priority mode, or Polled mode), the Interrupt Controller may not be able to determine the last interrupt acknowledged. In this case, a Specific EOI command must be issued that includes as part of the command the IS bit to be reset. A Specific EOI command is issued by writing a 6X hex to Port FFF0 with the least significant nibble of the byte indicating (in binary) the number of the IS bit to be reset.

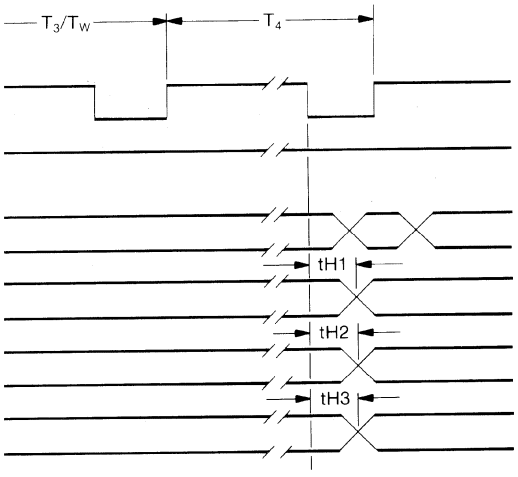
It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a Nonspecific EOI if the Interrupt Controller is operating in the Special Mask mode.

Automatic End of Interrupt (AEOI) Mode

If a 03 hex has been written to ICW4 during initialization, the Interrupt Controller operates in AEOI mode continuously unless the initialization sequence is repeated with ICW4 = 01 hex. In AEOI mode, the Interrupt Controller automatically performs a Nonspecific EOI operation at the end of the 8088 interrupt acknowledge cycle. Note that this mode should be used only when a nested multilevel interrupt structure (i.e., lower priority interrupts inhibited and higher priority interrupts enabled during an interrupt service routine) is not required since the IS bit of any interrupt is, in effect, cleared as soon as the interrupt is acknowledged.

Automatic Rotating Priority Mode — Equal Priority Interrupts

In some applications, it may be desirable to consider all possible 7864 interrupt sources as having equal priority. In this mode an interrupt, after being serviced, is redefined as having the lowest priority. Thus, any 7864 interrupt source requesting service has to wait, worst case, until each of the other seven interrupts have been serviced at most once. Figure 3-15 shows the priority and "in service" status before and after automatic rotation.



	4.9152 MHz		
	MIN	TYP	MAX
		203	
	133	135	137
	66	68	70

	4.9152 MHz	
	MIN	MAX
	61	
		102
		125
		57
		57
		57
	12	
	12	
	4	
	69	
	67	

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EST

EST

EST

EST

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OCW3 (Figure 3-16)

This control word enables or disables the Special Mask and Polled modes and selects which Interrupt Controller status register will be read from input port FFF1. OCW3 commands are issued by writing a byte having D3 set to 1, to Port FFF0.

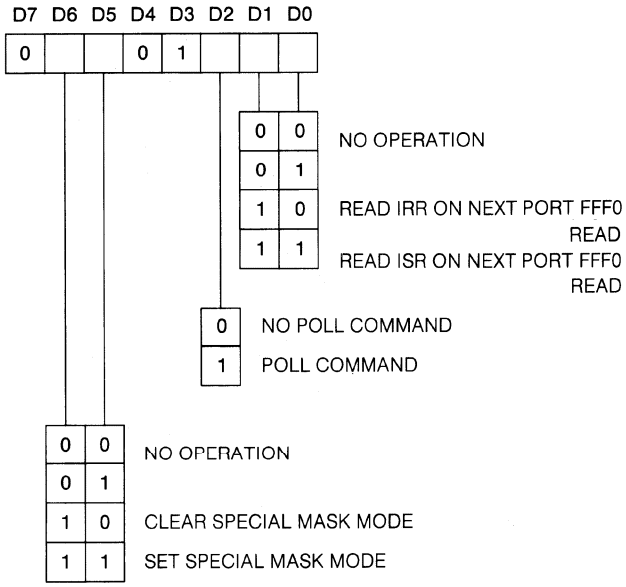
D7 D6 D5 D4 D3 D2 D1 D0
0 0 1
0 0 NO OPERATION
0 1
1 0 READ IRR ON NEXT PORT FFF0 READ
1 1 READ ISR ON NEXT PORT FFF0 READ
0 NO POLL COMMAND
1 POLL COMMAND
0 0 NO OPERATION
0 1
1 0 CLEAR SPECIAL MASK MODE
1 1 SET SPECIAL MASK MODE

Figure 3-16. OCW3 (Output Port FFF0 Hex)

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the Interrupt Controller priority structure during execution. For example, it may be necessary to inhibit lower priority interrupt requests for some portion of the interrupt service routine, but to enable some or all of them during another portion. The difficulty here is that if an interrupt request has been acknowledged but an EOI command has not yet reset its IS bit (i.e., during execution of the interrupt service routine), the Interrupt Controller inhibits all lower priority requests.

In this situation, the Special Mask mode may be used. In this mode, when a mask bit is set in OCW1, it inhibits further interrupts from that IR input and enables all other IR interrupts (both lower and higher priority) that are not also masked. Thus, any interrupts may be selectively enabled by loading the mask register.

The Special Mask mode is enabled by writing 68 hex to Port FFF0 and cleared by writing 48 hex to Port FFF0.

Section 4
OPERATING SOFTWARE

The 7864 onboard peripherals (Counter/Timer and Interrupt Controller) are initialized and operated by reading and writing the appropriate command, control, and data bytes to and from I/O ports. These operations are described in Section 3. The user can include output and input instructions (8088 instructions OUT, OUTS, or IN) as needed in the application program. Care should be taken to follow the programming instructions in Section 3 regarding port addresses, the command, control, or data bytes required, and the order in which they must be written and/or read.

Section 5
MAINTENANCE

REFERENCE DRAWINGS

The schematic (Figure 5-1) and assembly drawing (Figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

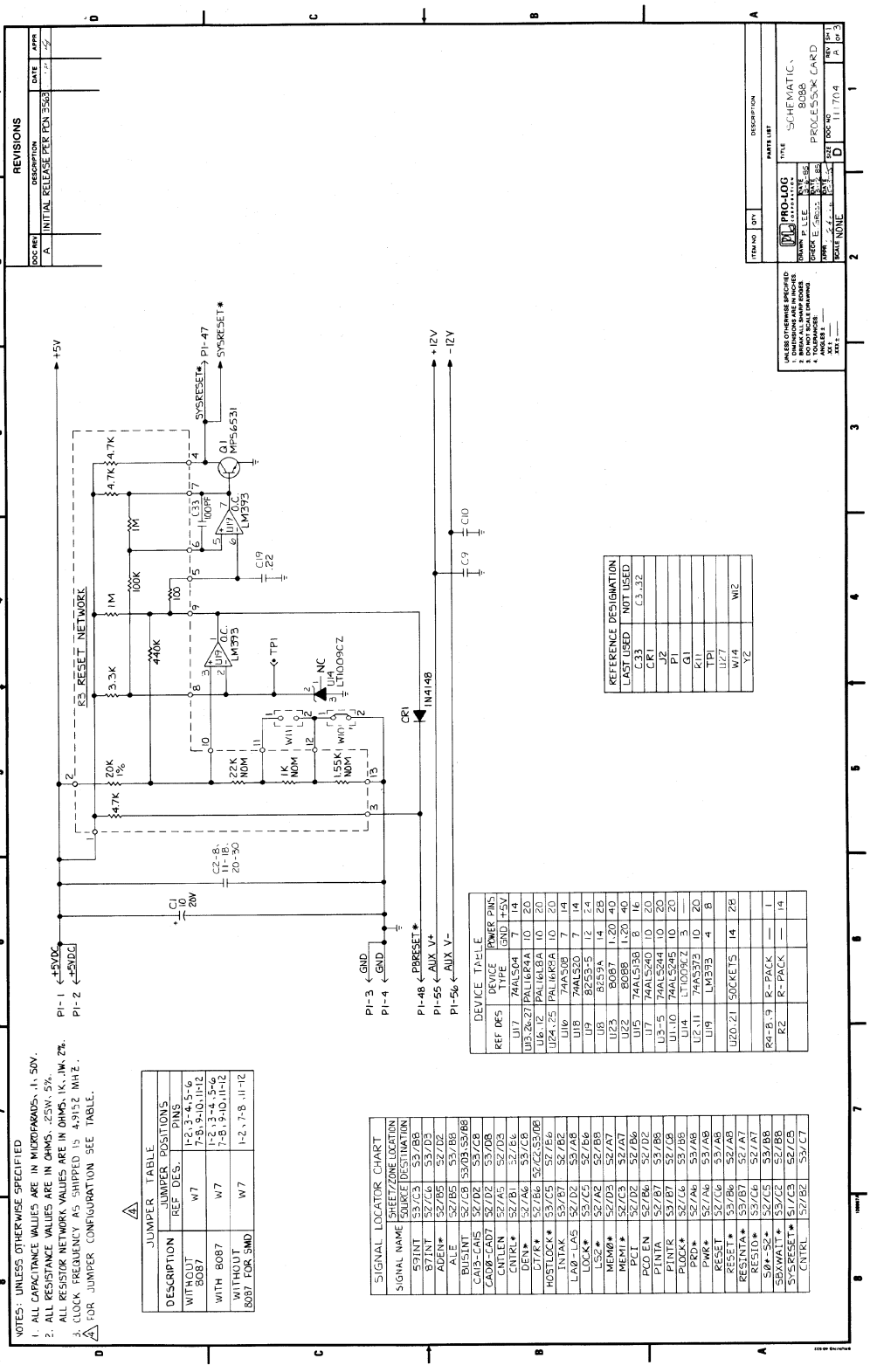
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±1, 50V.
2. ALL RESISTANCE VALUES ARE IN OHMS, .25W, 5%.
ALL RESISTOR NETWORK VALUES ARE IN OHMS, 1K, .1W, 2%.
3. CLOCK FREQUENCY AS SHIPPED IS 4.9152 MHZ.
4. FOR JUMPER CONFIGURATION SEE TABLE.
REVISIONS
DOC REV | DESCRIPTION | DATE | APPR
A | INITIAL RELEASE PER PCN 3563
JUMPER TABLE
DESCRIPTION | JUMPER POSITIONS REF DES. | PINS
WITHOUT 8087 | W7 | 1-2, 3-4, 5-6 7-8, 9-10, 11-12
WITH 8087 | W7 | 1-2, 3-4, 5-6 7-8, 9-10, 11-12
WITHOUT 8087 FOR SMD | W7 | 1-2, 7-8, 11-12
SIGNAL LOCATOR CHART
SIGNAL NAME | SHEET/ZONE LOCATION SOURCE | DESTINATION
S3INT | S3/C3 | S3/B8
B7INT | S2/C6 | S3/D3
ADEN* | S2/B5 | S2/D2
ALE | S2/B5 | S3/B8
BUSINT | S2/C8 | S3/D3,S3/B8
CAI3-CAI5 | S2/D2 | S3/C8
CA00-CA07 | S2/D2 | S3/D8
CNTLEN | S2/A5 | S2/D3
CNTRL* | S2/B1 | S2/E6
DEN* | S2/A6 | S3/C8
DTR* | S2/B6 | S2/C2,S3/D8
HOSTLOCK* | S3/C5 | S2/E6
INTAK | S3/B7 | S2/B2
LA0-LA5 | S2/D2 | S3/A8
LOCK* | S3/C5 | S2/E6
MSC* | S2/A2 | S2/B8
MEMW* | S2/D3 | S2/A7
MEMR* | S2/C3 | S2/A7
PCE | S2/D2 | S2/B6
PCLEN | S2/B4 | S3/D2
PINTR | S2/B7 | S2/C8
PIOR* | S3/D5 | S3/B8
PIOW* | S2/A6 | S3/A8
PWR* | S2/A6 | S3/A8
RESET | S2/C6 | S3/A6
RESET* | S3/B6 | S2/A8
RESINTA* | S3/B7 | S2/A7
RESIO* | S3/C6 | S2/A7
S0*-S2* | S2/C5 | S3/B8
SBXWAIT* | S3/C2 | S2/B8
SYSRESET* | S1/C3 | S2/C5
CNTRL | S2/B2 | S3/C7
DEVICE TABLE
REF DES | DEVICE TYPE | POWER PINS GND | +5V
U17 | 74ALS04 | 7 | 14
U3,26,27 | PAL16R4A | 10 | 20
U6, 12 | PAL16L8A | 10 | 20
U24, 25 | PAL16R8A | 10 | 20
U16 | 74AS08 | 7 | 14
U18 | 74ALS20 | 7 | 14
U9 | 8253-5 | 12 | 24
U8 | 8259A | 14 | 28
U23 | 8087 | 1,20 | 40
U22 | 8088 | 1,20 | 40
U15 | 74ALS138 | 8 | 16
U7 | 74ALS240 | 10 | 20
U3-5 | 74ALS244 | 10 | 20
U1,10 | 74ALS245 | 10 | 20
U14 | LTC09CZ | 3 | —
U2,11 | 74AS373 | 10 | 20
U19 | LM393 | 4 | 8
U20,21 | SOCKETS | 14 | 28
R4-8, 9 | R-PACK | — | 1
R2 | R-PACK | — | 14
REFERENCE DESIGNATION
LAST USED | NOT USED
C33 | C3,32
CR1
J2
P1
Q1
R11
TP1
U27
W14 | W12
Y2
P1-1 ←+5VDC
P1-2 ←+5VDC
P1-3 ←GND
P1-4 ←GND
P1-48 ←PRESET*
P1-55 ←AUX V+
P1-56 ←AUX V-
+5V
+12V
-12V
SYSRESET*→P1-47
SYSRESET*
R3 RESET NETWORK
4.7K
20K 1%
3.3K
440K
1M
100K
100
22K NOM
1K NOM
1.55K NOM
W11
W10
W12
C1 10 20V
C2-8, 11-18, 20-30
C19 .22
C33 100PF
C9
C10
CR1 IN4148
Q1 MPS6531
U14 LTC09CZ NC
U19 LM393
TP1
PROLOG
SCHEMATIC, 8088 PROCESSOR CARD
DOC NO 111704
REV A
SHT 1 OF 3
SCALE NONE
SIZE D

Figure 5-1. Schematic (Page 1 of 3)
FOR REFERENCE ONLY

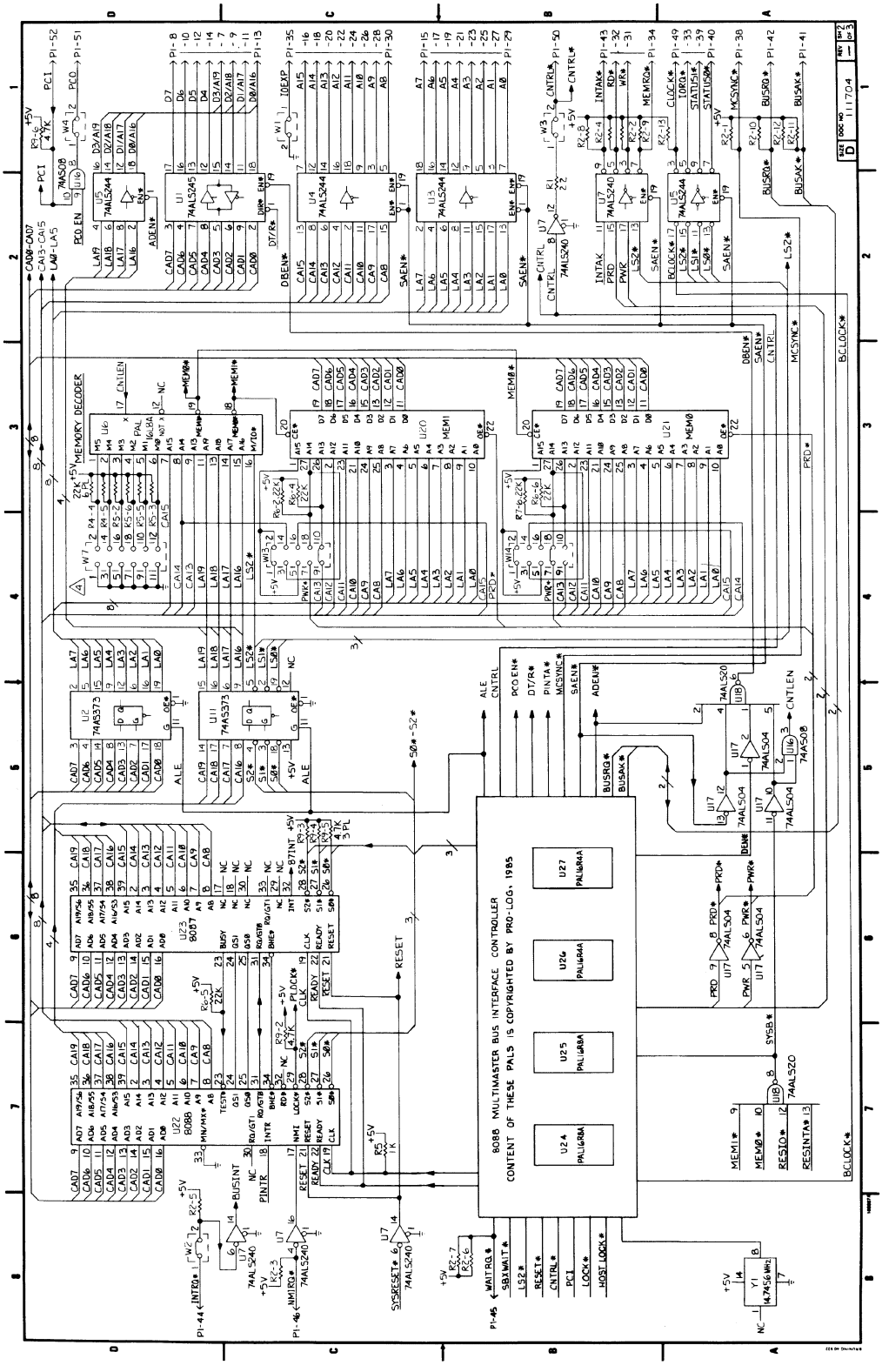

Figure 5-1. Schematic (Page 2 of 3)
FOR REFERENCE ONLY

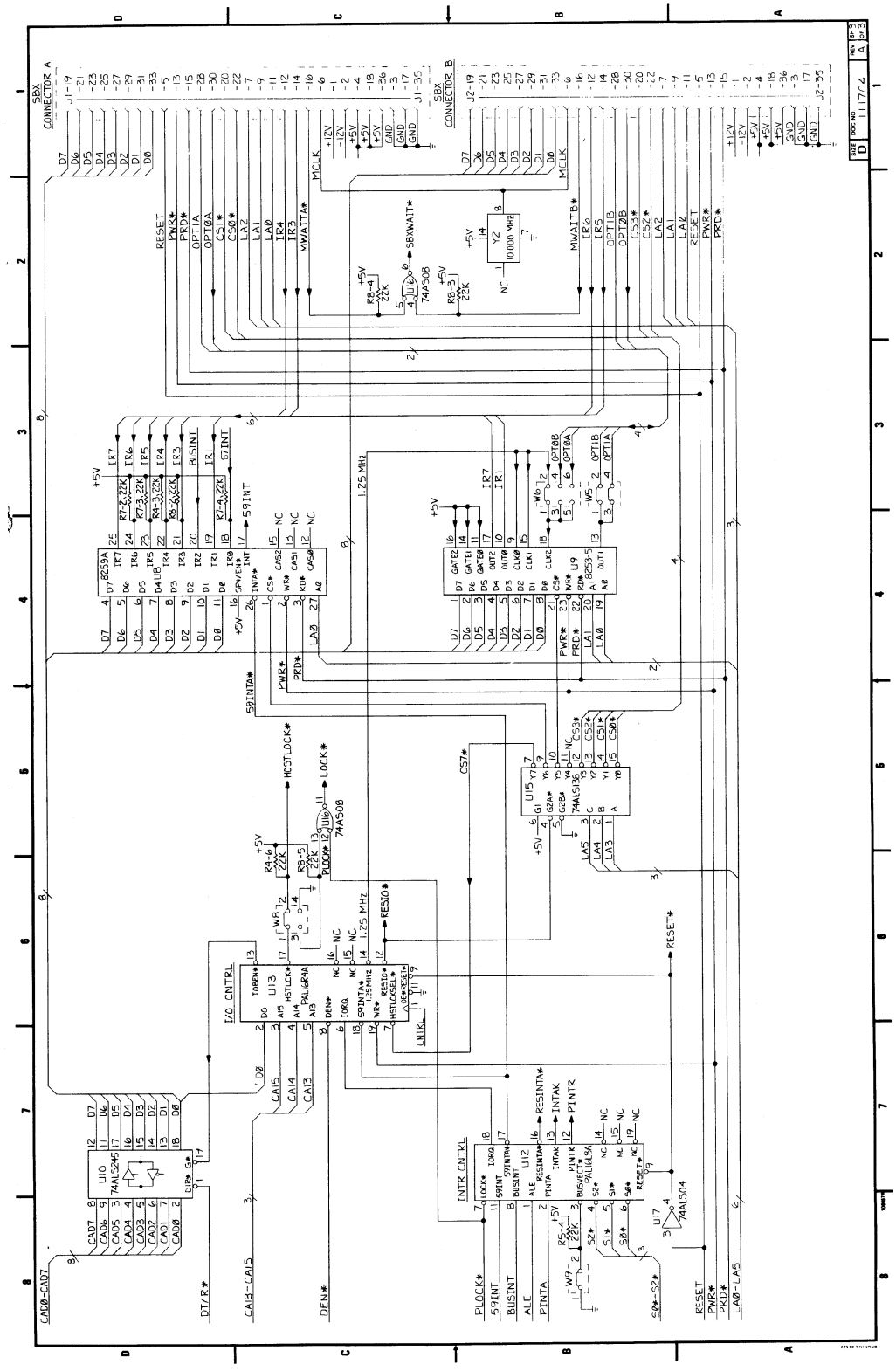

Figure 5-1. Schematic (Page 3 of 3)
FOR REFERENCE ONLY

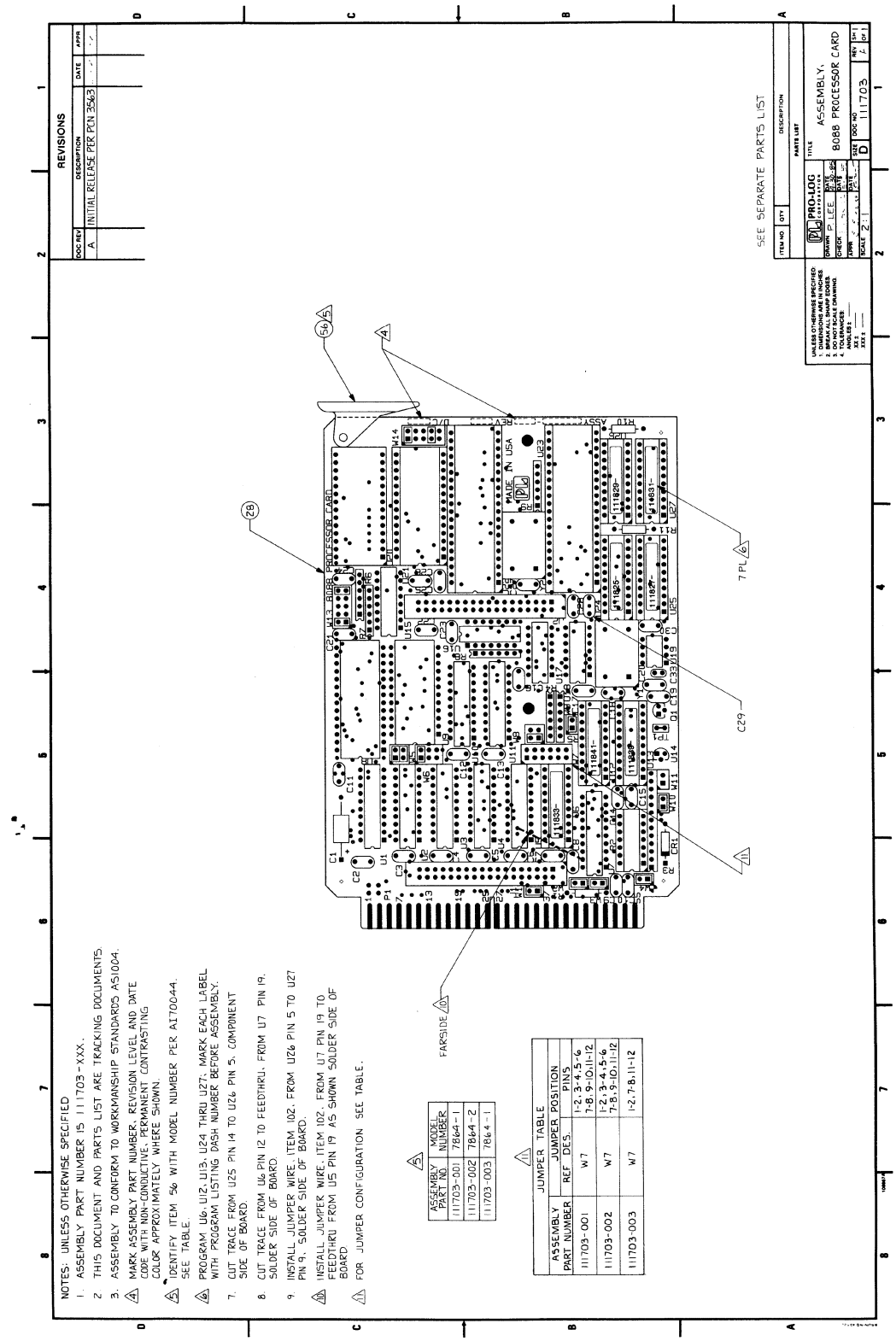

Figure 5-2. Assembly Drawing
FOR REFERENCE ONLY

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call Customer Support at (800) 538-9570, ext. 3617. In California call (408) 646-3617 from 7 a.m. to 4 p.m. (Pacific Time).
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

CAUTION

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2560 Garden Road
   Monterey, California 93940

   Reference CRO #_____

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment on PROM Programmers and STD BUS Series 7000 cards. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller of the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

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PRO-LOG® CORPORATION

Yes, I'm interested in Pro-Log.

Please send me more information about your:

- ☐ 7000 Series STD BUS Cards
- ☐ STD BUS Packaging Solutions
- ☐ STD BUS Subsystem
- ☐ STD BUS Systems
- ☐ Designer Software
- ☐ Design Courses and Seminars
- ☐ Programmer Product Line
- ☐ Other _____

- ☐ I am currently using Pro-Log equipment.
- ☐ Add my name to your mailing list.
- ☐ Please have a Sales Representative contact me.

Reader Comments:

Name _____ City _____

Company _____ State _____ Zip _____

Address _____ Telephone _____

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CORPORATION

2560 GARDEN ROAD
MONTEREY, CA 93940

Attn: Literature Department